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Experimental Study of the Equalization Requirements of a 2.5D Co-Packaged 16-nm CMOS Optical Receiver up to 160 Gb/s

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Abstract *We demonstrate the DSP-based feed-forward and decision-feedback equalization requirements in 2.5D co-packaged CMOS optical receivers. Experimental results confirm optical reception up to 160-Gb/s/λ PAM-4 and 90-Gb/s/λ NRZ signaling with a bandwidth-limited prototype comprised of a TIA in 16-nm FinFET CMOS co-packaged with a commercial photodiode. ©2022 The Author(s)*

Introduction

Ethernet standards, such as PAM-4 800G-DR8 and 400G-DR4/FR4 for intra-data center links with intensity-modulation direct-detection (IM/DD) systems, require the design of energy-efficient and low-cost optical receivers supporting data rates exceeding 100 Gb/s/λ[1],[2]. While SiGe BiCMOS technologies offer high gain and low noise optical receivers[3],[4], advanced CMOS technologies allow the integration between the optical receivers and the host SerDes on the same chip while offering good switching characteristics with high energy efficiency[5]. This can be leveraged in the design of low-cost and high-density receivers that use equalization implemented in digital-signal-processing (DSP) to achieve higher data rates[6],[7]. Such optical receiver comprising a transimpedance amplifier (TIA) followed by ADC and DSP are shown in Fig. 1.

Traditional optical receivers with TIA in the front-end are designed to have bandwidths (BWs) in the range of $0.5-0.7\times$ of baud rate. However, at data rates exceeding 150 Gb/s, achieving the required BW comes with the cost of heavily reduced transimpedance. This leads to degraded sensitivity, higher thermal noise, and higher power[8]. To overcome this trade-off, the TIA BW can be intentionally limited to below $0.5\times$ baud rate, allowing for increased transimpedance at the cost of the intersymbol interference (ISI)[9]. ISI can then be removed with widely adapted, DSP-compatible, and CMOS suitable equalization techniques that are the feed-forward equalizer (FFE) and the decision feedback equalizer (DFE)[10]. Several state-of-the-art CMOS optical receivers[11],[12] have used such approach but the equalization taps were limited to a few. Many recent works have also demonstrated 100+Gb/s with sophisticated DSP approaches which can entail much higher silicon area and power[13]–[15]. However, the study of DSP requirements and its full potential with simple equalization strategies such as FFE and DFE are not yet clear[16], especially in co-packaged CMOS optical receiver system performing at such high data rates.

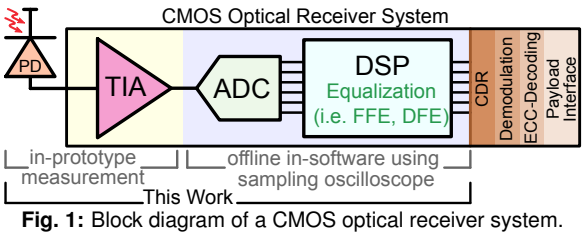


Fig. 1: Block diagram of a CMOS optical receiver system.

For higher data rate operation with a limited-BW receiver, it is crucial to appropriately select the number and the combinations of FFE (i.e. pre-cursors and post-cursors) and DFE taps. This work, demonstrates up to 160 Gb/s PAM-4 optical data reception with a co-packaged CMOS optical receiver with a limited BW of 32 GHz while reporting the DSP-based FFE and DFE equalization requirements.

Simulated Equalization Requirements

To highlight the FFE/DFE requirements at such datarates, we study the vertical-eye-opening (VEO) across various combinations of FFE and

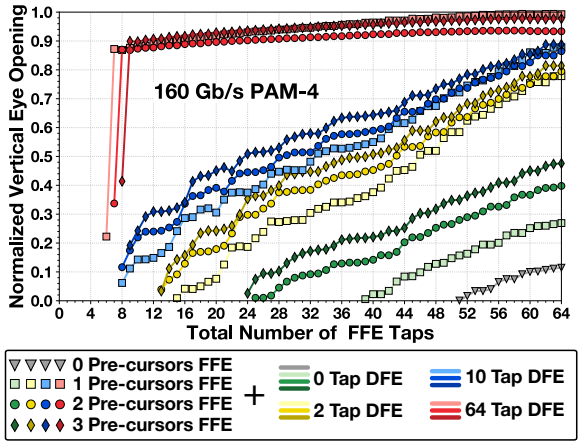


Fig. 2: Simulated VEO as a function of the total number for FFE taps across various combinations of FFE pre-cursor taps and DFE taps at 160 Gb/s PAM-4.

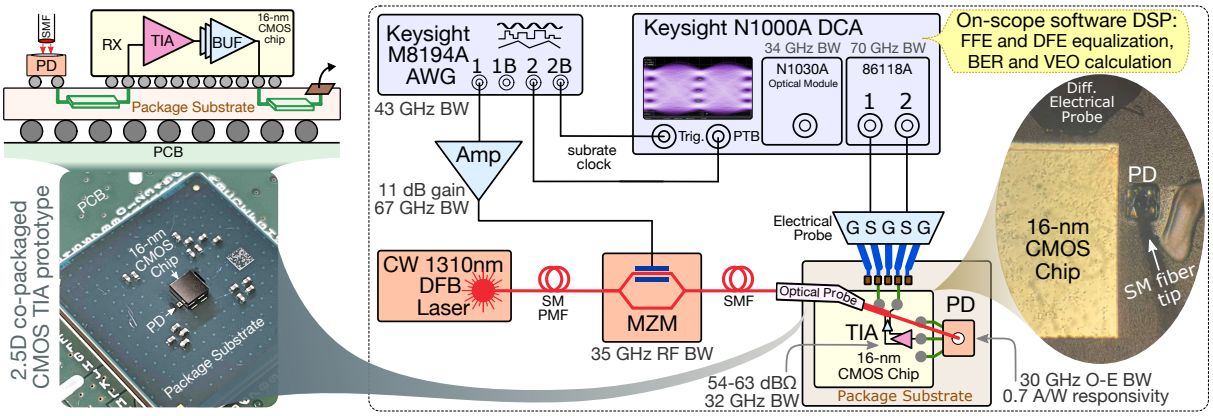


Fig. 3: Measurement setup to study the FFE/DFE equalization requirements in 2.5D co-packaged CMOS optical receivers.

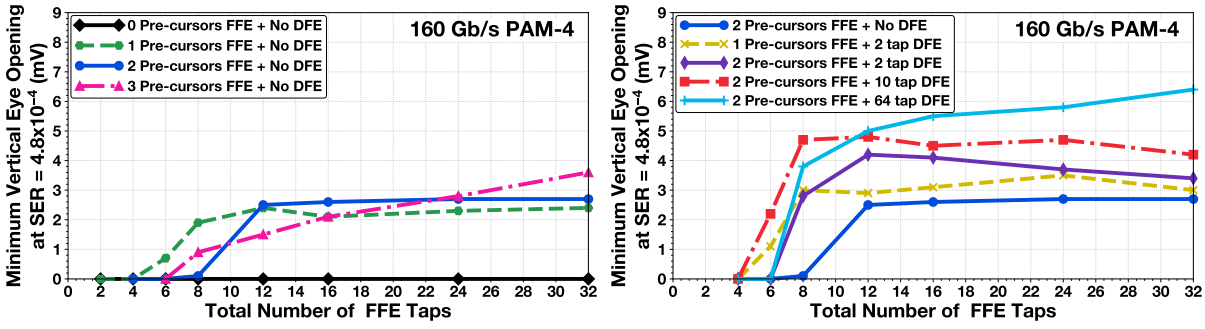
DFE taps. Fig.2 shows the simulated worst-case VEO as a function of total number of FFE taps across various combinations of pre-cursor FFE taps and DFE taps at 160 Gb/s PAM-4. Worst-case VEO is computed using peak-distortion analysis[17] after processing the pulse response through in-software FFE/DFE with optimized tap coefficients. The pulse response is obtained from the measured transimpedance response from our recent work[18]. As can be seen with the case of 0 tap DFE, having more pre-cursor FFE taps leads to significantly improved VEO with diminishing return after 2 pre-cursor taps. Moreover, adding more DFE taps for a given number of FFE taps always leads to improved VEO. We further demonstrate this study with measurements.

Experimental Setup

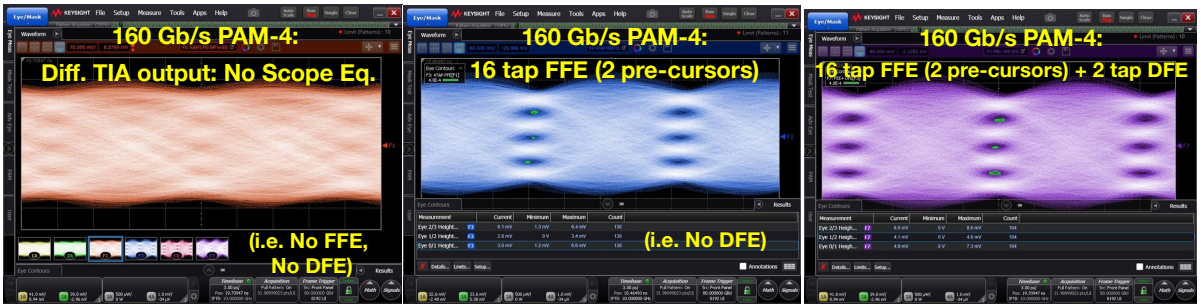
Fig .3 shows the optoelectrical measurement setup. A lensed single-mode fiber tip is used to free-space couple the modulated optical signal (λ=1310 nm) onto the back-illuminated PD (30 GHz O-E BW and 0.7 A/W responsivity) with flip-chip 2.5D co-packaged 16-nm FinFET CMOS TIA prototype with 32 GHz BW described in our recent work[18]. Differential TIA outputs are electrically probed and captured by a sampling oscilloscope which performs the desired FFE and DFE equalization with optimum tap coefficients mimicking the ADC and DSP blocks from Fig. 1.

Experimental Results and Discussions

160 Gb/s PAM-4 measurements are performed with QPRBS13 pattern with input optical modulation amplitude (OMA) of -4.24 dBm, extinction ratio (ER) of 1.26 dB, and TIA gain set at 60 dBΩ. Minimum VEO at symbol-error-rate (SER) of 4.8×10^{-4} (pre-FEC limit[1]) is measured. Fig .4a shows the resulting VEO across the total number of FFE taps for a different number of pre-



(a) (b)



(c) (d) (e)

Fig. 4: Measured VEO at 160 Gb/s PAM-4 with (a) FFE only (b) FFE + DFE. Eye diagrams of (c) TIA output without FFE or DFE (d) with 16 tap FFE (2 pre-cursor) (e) with 16 tap FFE (2 pre-cursor) + 2 tap DFE.

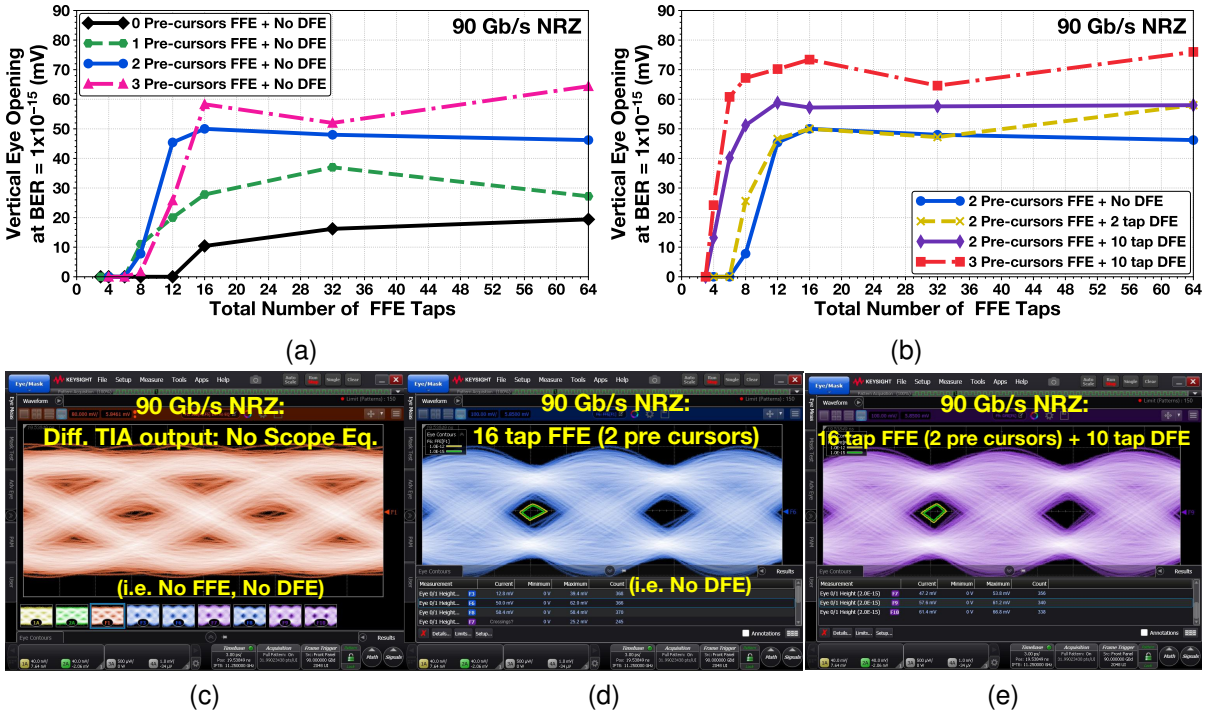


Fig. 5: Measured VEO at 90 Gb/s NRZ with: (a) FFE only (b) combinations of FFE + DFE. Measured eye diagrams of: (c) TIA output without equalization (no FFE/DFE) (d) with 16 tap FFE (2 pre-cursors) (e) with 16 tap FFE (2 pre-cursors) + 10 tap DFE.

cursors. Measurements reveal that at least one pre-cursor tap is required to open the eye (i.e., VEO$>$0) with diminishing return after 2 pre-cursor FFE taps. Fig.4b shows the VEO when DFE is enabled along with FFE. It clearly emphasizes that having more DFE taps further improves the VEO, albeit with a diminishing improvement for DFE taps greater than 10 taps. Resulting eye diagrams of the prototype outputs without any equalization is shown in Fig.4c followed by the DSP processed eye-diagrams after enabling total of 16 tap FFE (2 pre-cursor taps) with no DFE and 16 tap FFE (2 pre-cursor taps) + 2 tap DFE illustrated in Fig. 4d, and Fig.4e, respectively.

Experiment is further performed for 90 Gb/s NRZ with required bit-error-rate (BER)$<1\times10^{-15}$ targeted for low-latency optical receivers (i.e. no forward-error-correction is tolerable). Measurements are executed with a PRBS11 pattern with -4.37 dBm input OMA, 1.25 dB ER and 63 dBΩ gain in TIA. As shown in Fig. 5a, for a given number of FFE taps, as the number of pre-cursor taps is increased, VEO is improved; again with the diminishing return for pre-cursor taps greater than 2. Moreover, adding DFE taps further improves VEO as shown in Fig.5b. To show this trend, captured eye diagrams with three different equalization settings are shown in Figs.5c, 5d and 5e.

Note that the VEO increases sharply with the total number of FFE taps up to roughly 12 taps since ISI is dominant and additional equalization significantly improves VEO. As the total number of FFE taps grows beyond 12 taps, all possible improvement from equalizing BW limitations and reflections has already been achieved so the VEO approaches a relatively constant value. Thermal noise then limits the performance resulting in small variations in measured VEO for total number of FFE taps more than approximately 12 taps.

Conclusion

We have experimentally demonstrated 160 Gb/s PAM-4 and 90 Gb/s NRZ optical data reception while highlighting the importance of pre-cursor FFE taps, the total number of FFE taps and DFE taps for a 2.5D co-packaged CMOS optical receiver prototype with a limited TIA BW of 32 GHz and a PD BW of 30 GHz. Notably, at least 12 total FFE taps with minimum of 2 precursor taps in combination with 2-to-10 DFE taps were required to achieve near-optimum performance. ADC-based co-packaged CMOS optical receivers can leverage this simple digital equalization approach to achieve data rates required by the 400G/800G and emerging 1.6T Ethernet standards.

Acknowledgement

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