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# Fully Integrated Silicon Photonic Circuit technology with SiN passives, Ge photodetectors and III-V/Si SOAs

Martin Peyrou[(1)], Jason Mak[(1)], Torrey Thiessen[(1)], Kevin Froberger[(1)], Florian Denis-Le Coarer[(1)], Zheng Yong[(1)], Laurent Milord[(1)], Marylise Marchenay[(1)], Frédéric Mazur[(1)], Yannis Le Guennec[(2)], Christophe Jany[(3)], Joyce K.S. Poon[(4,5)], and Sylvie Menezo[(1)]

[(1)] SCINTIL Photonics, 7 Parvis Louis Néel, 38040 Grenoble, France, sylvie.menezo@scintil-photonics.com
[(2)] GIPSA-lab, 11 Rue des Mathématiques, 38400 Saint-Martin-d'Hères, France
[(3)] CEA-LETI, 17 rue des Martyrs, 38000 Grenoble, France
[(4)] University of Toronto, Department of Electrical and Computer Engineering, 10 King's College Road, Toronto, ON M5S 3G4, Canada
[(5)] Max Planck Institute of Microstructure Physics, Weinberg 2, 06120 Halle (Saale), Germany

**Abstract** *We present for the first time a fully integrated silicon photonic circuit technology. III-V on Si amplifiers are monolithically integrated at the backside of advanced Silicon photonic wafers comprising SiN passive devices, Si based phase shifters and Ge waveguide-photodetectors.*

## Introduction

Monolithic heterogeneous integration of III-V components onto Silicon (Si) has been mastered by bonding III-V dies and patterning them at the wafer-level to produce multiple integrated lasers or Semiconductor Optical Amplifiers (SOA) with best-in-class performances [1]. Compared to platforms based on external grating or butt-coupled lasers, heterogeneous integration offers wafer-scale CMOS manufacturing and testing. Co-integration of transmitter (Tx) and receiver (Rx) components is essential to the extensive parallelism demanded in next generations of optical communications and sensing applications. For example, future short reach transceivers will most likely parallelize 8 to 16 x 100 Gbit/sec to 200 Gbit/sec Tx and Rx, and sensing applications such as Frequency Modulated Continuous Wave (FMCW) LIDAR rely on multiple I/Os [2]. Co-integration of Tx and Rx is needed to reduce the assembly steps and related optical and electrical packaging losses.
In [3], III-V/Si waveguide-photodetectors (PD) were reported to be monolithically integrated with a laser using the same III-V stack. The use of Germanium (Ge) waveguide-PD featuring high responsivity in O and C bands, compactness and therefore ultra-highspeed [4] would be a key advantage.

We report here, for the first time to our knowledge, on the monolithic integration of III-V/Si SOAs, Ge waveguide-PDs, Si active and Silicon Nitride (SiN) passive devices, using a demonstration photonic integrated circuit (PIC) at 1550 nm. The 'demo' circuit intended to be used in a FMCW LIDAR system comprises SiN Multi Mode Interferometers (MMI) and crossings, doped Si Phase Shifters (PS), Ge waveguide-PDs and III-V/Si SOAs. The performance of each individual integrated component is measured using dedicated on chip test structures.

## Technology platform

The wafer-level CMOS fabrication process of our integrated circuit technology was previously reported in [5], where multiple III-V based devices are patterned on a III-V material-stack bonded at the backside of a Si photonic base wafer (Backside-On-BOX photonic integrated circuit technology). The Si photonic wafer is made from standard Si Photonics processes and can comprise Si and SiN passive components, Ge waveguide-PDs and doped Si based active devices (for high or low speed phase shifters). Fig.1 shows a schematic cross section of a III-V/Si SOA, Si/SiN waveguides and a Ge waveguide-PD built according to such integration process.

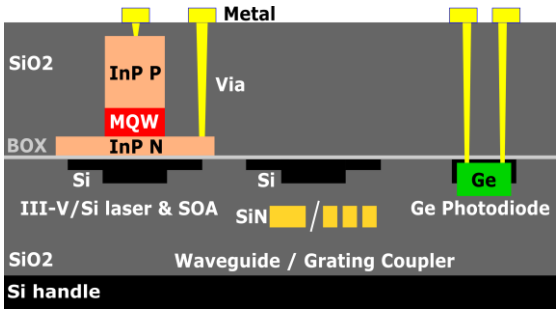


**Fig. 1:** Cross section of the 'Backside on Box integrated circuit technology'.

## Demonstration PIC

Our demonstration PIC for use in an FMCW LIDAR system is described in Fig. 2. The PIC comprises a Tx and Rx tile. The circuit is intended

to be fed by an external laser through a SiN surface grating coupler (GC in). Following the GC, a 'booster SOA is monolithically integrated on chip. A SiN 1×2 MMI splits the amplified signal into a first part to form a local oscillator (LO) and a second part directed to a SiN GC ('GC Tx out') for ranging a non-represented target. The Rx comprises a SiN GC ('GC Rx in') port to collect the signal reflected. The latter is mixed on-chip with the LO onto the coherent receiver which comprises 2×2 SiN MMI, SiN crossings and a pair of Ge balanced PDs. Not represented in Fig. 2, nor integrated onto our 'demo PIC', the Rx tile can also comprise:

- a low-speed phase shifter (PS) made from a doped-Si waveguide, to correct phase errors related to fabrication variations,
- a 'preamplifier SOA' prior to being mixed with the LO on the receiver block.

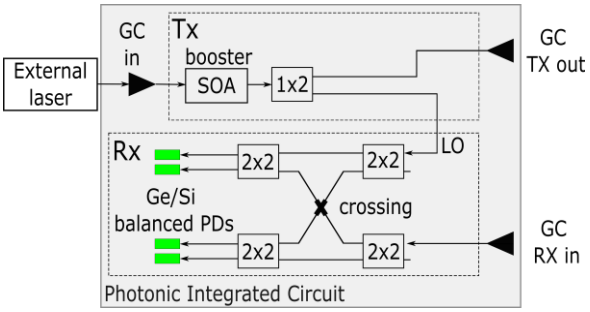


**Fig. 2:** FMCW LIDAR core circuit architecture

**Performance of each individual components**

To test each individual integrated component, we designed and used dedicated test structures.

We first start by measuring the transmission loss of two connected SiN GCs. Fig. 3 reports on the measurements made over twelve dies (the Insertion Loss -IL- of one single SiN GC is obtained by dividing by two). This measurement enables to further de-embedded the IL of the other characterized components.

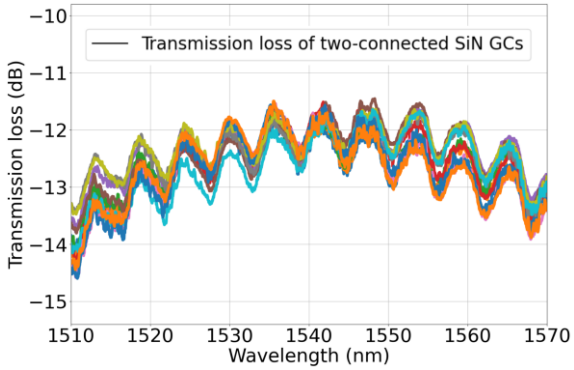


**Fig. 3:** Transmission loss of two-connected SiN GCs over 12 dies.

The IL of the 2×2 SiN MMI is reported in Fig. 4 after removing the GC losses previously measured. The MMIs are balanced within +/- 0.5dB over the 1510-1570 nm wavelength range.

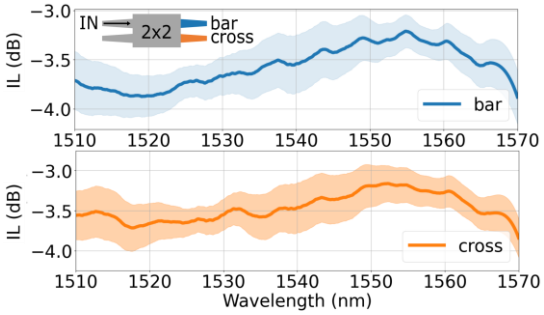


**Fig. 4:** Measured IL over 12 dies of the SiN 2×2 MMI.

The crossings' measured loss was below 0.35 dB over the same wavelength range.

The waveguide Ge PDs were tested as single PDs waveguide-coupled to a SiN GC. Their width and length are respectively 8 µm-wide and 45 µm-long. The PD dark current ranges from 8 nA at -0.1 V to 290 nA at -2 V. The Ge PDs responsivity against wavelength is shown in Fig. 5 for several reverse bias voltages, subtracting the loss of the coupling GC. At 1510 nm, it reaches 0.9 A/W.

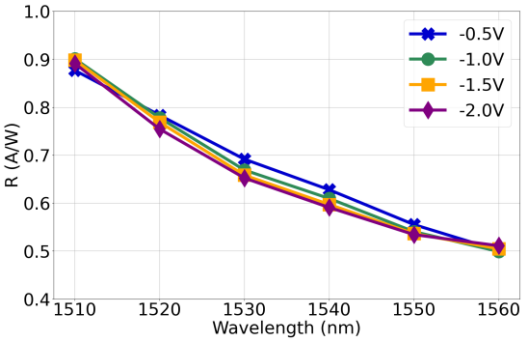


**Fig. 5:** Ge photodiode responsivity as a function of wavelength for several reverse bias.

To characterize the low-speed doped Si PS, we embedded them in Mach-Zehnder Interferometers (MZI). A $\pi$ phase shift required applying 86 mW of electrical power on the PS.

The SOA gain was measured using the dedicated on-chip test structure of Fig. 6.

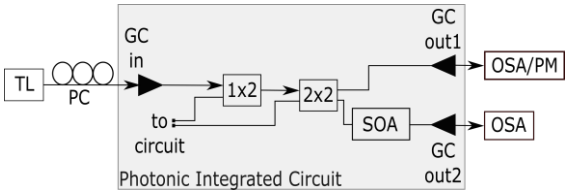


**Fig. 6:** Dedicated test structure for the measurement of SOA gain. OSA: Optical Spectrum Analyzer, PM: Power meter

A tunable laser (TL) with a polarization controller (PC) is coupled to the SiN 'GC in' of the test

structure. We measured the transmission loss of the “reference” path (‘GC in’ to ‘GC out1’) and the “amplified” path (‘GC in’ to ‘GC out2’) comprising exactly the same components of the “reference” path, but with an SOA prior to the output GC.

Fig. 7 shows the measured transmission loss of the “reference” path over the 1510-1570 nm spectral range and at several chip temperatures using the power meter. As expected, negligible temperature dependence is observed as the ‘reference path’ comprises SiN passive components with temperature dependency <10pm/°C.

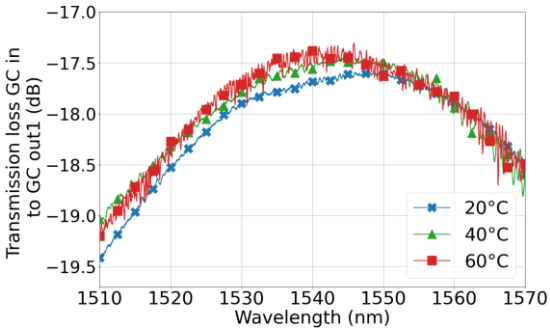


**Fig. 7:** Measured transmission loss of the “reference path” from (‘GC in’ to ‘GC out1’) at several chip temperatures

We then measured both the ‘reference’ and ‘amplified’ paths using the Optical Spectrum Analyzer (OSA). The SOA gain is extracted by measuring the power at the TL wavelength with and without the SOA. Fig.8 shows the measured gain against chip temperature at several wavelengths and SOA currents. Two SOA input optical power configurations were tested:

1) To investigate the SOA behaviour as a booster, we set the TL output power so that the input power of the integrated SOA reaches -2dBm (Fig. 8 top). At 20°C and 120 mA driving current, the SOA gain can be >10 dB from 1510 to 1550 nm. The gain decreases gradually as the chip temperature increases, down to ~5dB at 60 °C. Above 80 °C, the SOA shows no amplification at the measured wavelengths.

2) To assess the SOA behaviour as a preamplifier, we set the TL output power so that the input power of the integrated SOA reaches -20 dBm (Fig. 8 bottom). At 20°C and 120 mA driving current, the SOA gain can be >15 dB from 1510 to 1550 nm. The gain decreases gradually as the chip temperature increases, down to ~5dB at 60 °C.

The SOA voltage against current curves (VI curves) at the three temperatures are shown on Fig. 9, indicating that its power consumption for a 120 mA driving current is ~220 mW.

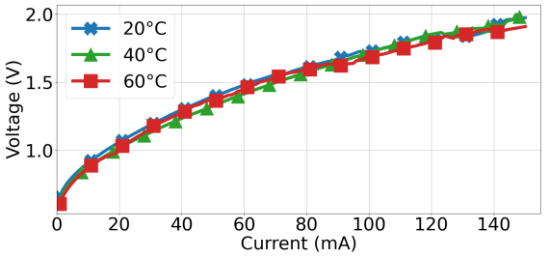


**Fig. 9:** SOA VI curves at 20 °C, 40 °C and 60 °C

## Conclusion

We presented for the first time, a fully integrated Silicon photonic technology that monolithically integrates III-V/Si SOA, Ge waveguide-PD and Si/SiN passive and active components. In future work we will report on the performance of the described and fabricated demo PIC.

## Acknowledgements

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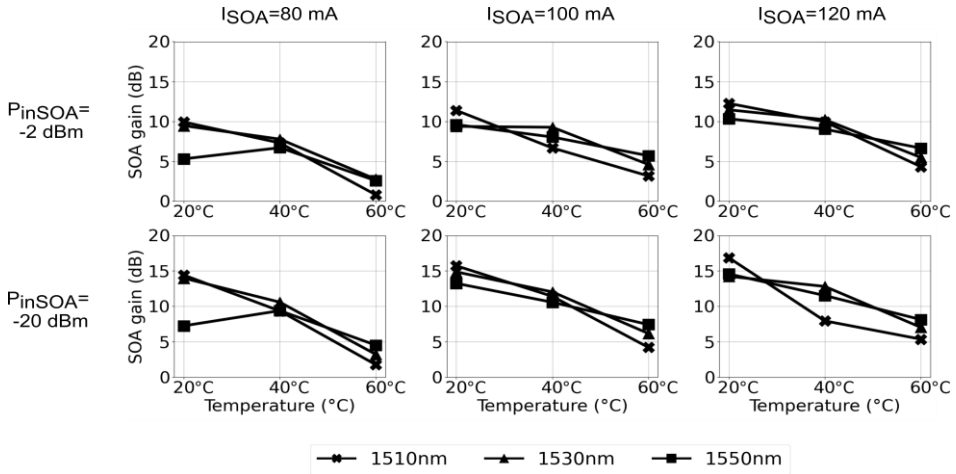


**Fig. 8:** SOA gain against chip temperature at 1510, 1530 and 1550 nm for 80 mA, 100 mA and 120 mA SOA currents. The SOA input power is set to -2dBm (top) and -20dBm (bottom)

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