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Experimental Demonstration of an All-Optical 2-bit Address Router Look Up Table

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Abstract *We experimentally demonstrate an all-optical 2-bit Address-Look Up table combining optical CAM and RAM tables with an optical Encoding/Decoding circuit. Error-free operation at 10Gb/s has been obtained for different CAM/RAM row contents.*

Introduction

The continuous growth of the connected devices number along with the vast computational demands, has led the Routing Information Tables (RIT) to follow a trend towards larger table entries, indicating a constant need for faster Header processing time for Address Lookup (AL) and information processing operations, that leads to major performance bottlenecks in network-operations [2]. Although AL tables, comprised of electronic Content Addressable (CAMs) and Random-Access Memories (RAMs), can comprehend intensive applications, allowing for fast AL operations, in a single clock cycle [3], their speed is limited due to the clock speed of the CAM, that rarely exceeds 1 GHz [4].

On the other hand, optical memory technologies have shown the potential to support high-speed data-rates, with photonic CAM and RAM cells [5][6], that can be utilized for fast AL router functionalities. Experimental demonstrations of optical CAM cells have indicated 10 times higher speeds than their electronic counterparts [7], allowing for Matchline (ML) schemes [6], that can look-up a destination address directly in the optical domain [8]. At the same time numerous novel optical RAM architectures [5], have already been demonstrated indicating complete single and multi-bit memory implementations [9], as well as Cache memory architectures [10], capable of performing high-speed data transfer and can be used for computing applications [11]. Moreover, a complete optical 2-bit CAM ML architecture, incorporating also Encoding and Decoding utilities has also been demonstrated [12], but still there has yet to be proposed an all-optical AL architecture, which includes a RAM table configuration, in order to trigger the matched CAM line output, accessing the proper RAM table entry for a complete routing operation [13].

In this work, we present for the first time, to the best of our knowledge, a complete optical AL architecture that can successfully identify 2-bit optical search words and correlate this with respective 2-bit router port address fields at 10Gb/s. The optical AL table employs an all-optical CAM and an all-optical RAM table connected via an optical Encoding/Decoding circuitry. Proof of principle experimental demonstration for different CAM/RAM memory contents and different CAM/RAM line configurations is reported using monolithically integrated InP Semiconductor Optical Amplifier (SOA)-based Flip-Flops (FFs) as its memory elements and SOA–Mach Zehnder Interferometer (MZI) gates for CAM search and RAM access circuitry, revealing error-free operation with a power penalty of ~9 dB at 10Gb/s.

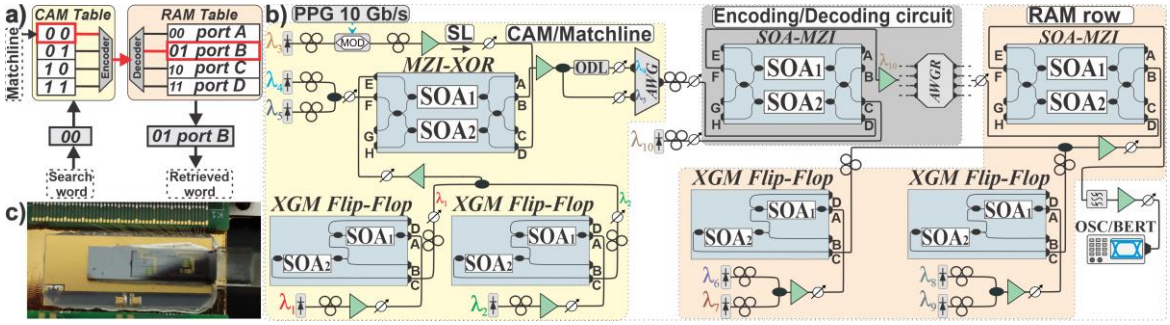

Fig. 1: (a) Schematic of AL table, (b) Experimental setup of the 2-bit complete AL operation and (c) Photo of the electro-optic packaged FF chip.

Experimental Setup

Fig. 1. (a) illustrates a conceptual schematic of an AL table when 2-bit values both for the search and retrieved words are used, with the search and retrieved words typically forming the destination address and the router output port address, respectively, within a router configuration. The incoming search word is simultaneously compared with every entry of the CAM table, generating a *"match"* signal only at the CAM row, that has an identical content. The *"match"* signal is then forwarded to the RAM table through an Encoding/Decoding circuit that is responsible for relating every *"match"* signal to the correct RAM row, which in turn stores the router output port address that has to be activated upon every "match" signal.

Fig.1. (b) depicts the experimental setup of the proposed 2-bit AL architecture. The two CAM cells comprise two discrete FFs that are responsible for storing the 2-bit content of every CAM row, following the principle and layout, described in [6]. Two CWs (λ_1, λ_2) at 1553.2 nm and 1547 nm, respectively, were fed as input light to the respective FFs and were used for setting the FF state at one of the two possible FF states with detailed description of the *Write* operation to define the state of the bistable photonic memory, found in [14]. The optical outputs of the two FF cells, were collected through port C and were then coupled together and inserted through port E into the SOA-MZI XOR gate. A CW signal generated at λ_3=1547.5 nm by a tunable laser source (TLS) was then modulated by a Ti:LiNbO$_3$ modulator at 10 Gb/s Programmable Pattern Generator (PPG) with NRZ 2^7-1 PRBS data streams. The λ_3 signal acts as the search signal, entering the optical XOR gate via port D, with the XOR input signals comprising two CW signals at λ_4=1546.3 nm and λ_5=1544 nm that were coupled together and inserted via port F. In this way, a single optical XOR gate was used to emulate the two respective XORs that would be required within a 2-bit CAM line, with the XOR output signals at λ_5 and λ_4 carrying the logical comparisons between λ_3 and λ_1 and λ_3 and λ_2, respectively.

Afterwards, the optical signals λ_5 and λ_4 were desynchronized and then multiplexed by the means of an AWG multiplexer, producing in this way a multi-level ML signal at the output of the AWG, that is forwarded to the Encoding/Decoding circuit, completing the CAM Matchline operation. The Encoding/Decoding operation was performed by an additional discrete SOA-MZI that acts as a wavelength converter. A tunable laser source emitting a CW signal at λ_{10} was used to provide the SOA-MZI input signal via its port C, with λ_{10} ranging between [1548.8-1551.2 nm] with a 0.8 nm step. In this way, the multi-level signal, that enters the SOA-MZI via its port D, gets converted into a binary NRZ waveform and wavelength-converted onto λ_{10}. This signal gets then forwarded to a 4-port AWGR, so that the wavelength converted *"match"* signal gets wavelength-routed to a specific output port and directed to the appropriate RAM row. As such, the CAM/RAM row mapping adopted in the router AL is configured by the exact λ_{10} wavelength value enforced at the SOA-MZI input. The memory cells of the RAM configuration were also based on two discrete FFs, along with another SOA-MZI AG that offers the RAM row Access functionality. Four CW signals, λ_6=1547.51 nm, λ_7=1549.31 nm, λ_8=1550.84 nm and λ_9=1552 nm, were also propagated as input light at the two RAM optical FFs. Specifically, λ_6 and λ_7 signals were fed to the FF via port D configured again to operate at one of the two optical FF states, and were collected at port C. The same principle was followed for the signals λ_8 and λ_9. The four signals were then

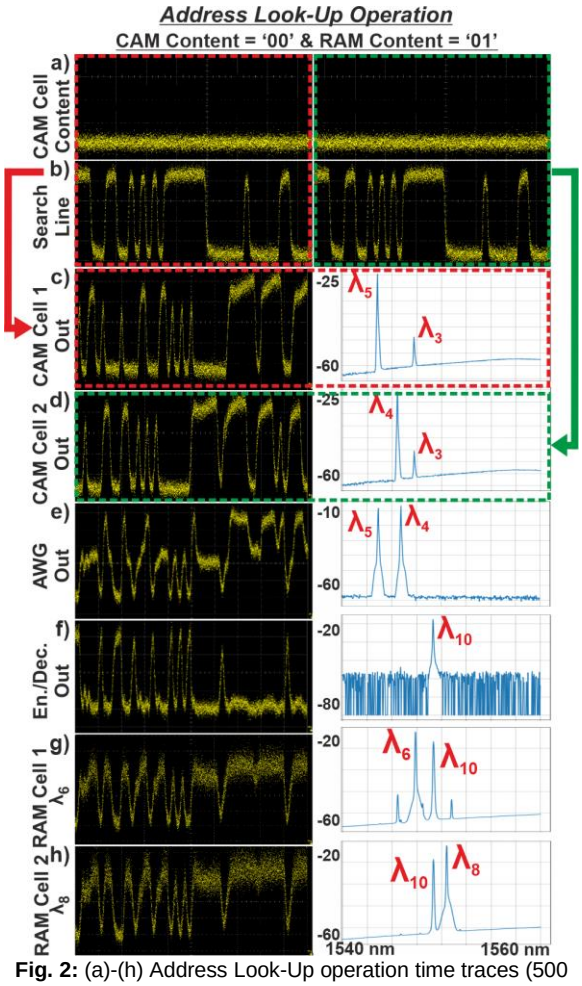

Fig. 2: (a)-(h) Address Look-Up operation time traces (500 ps/div) and spectra, for CAM content ='00' and RAM content = '01'.

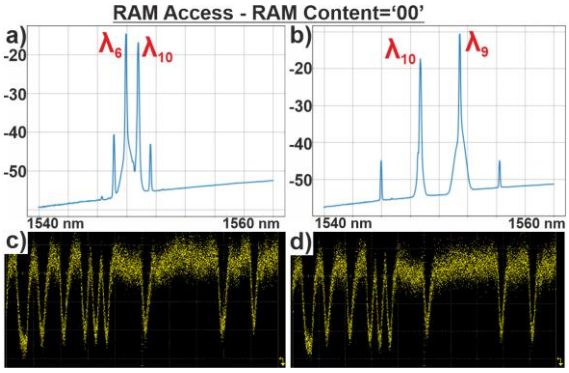

Fig. 3: (a)-(b) Output spectra for RAM content = '00', (c) Output trace for RAM content = '00', at λ_6 and (d) Output trace for RAM content = '00', at λ_8 dominant wavelength.

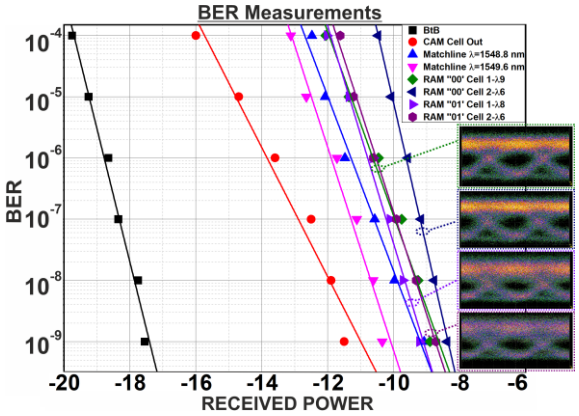

Fig. 4: BER curves for BtB, XOR, ML and RAM access operation, at 10 Gb/s.

coupled and propagated to the MZI-AG via port B, while the wavelength-converted λ_{10} signal, is being fed via port D, for the RAM access functionality. The output signal is collected at port F of the AG, concluding in this way the AL operation. EDFAs, VOAs, and PCs were used to tune the signals at around 1 dBm for λ_3, around 12 dBm for the λ_4 and λ_5 signals, 7 dBm for the multi-level signal, around -2 dBm for λ_{10} and around 1.5 dBm for the RAM signals. The FF SOAs were driven at 200 mA and around 260 mA and 250 mA for the MZI-XOR and MZI-AGs, respectively. Fig. 1. (c) shows a photo of one of the four monolithically integrated InP FF chips that were used as the memory cells in the CAM and RAM tables, fabricated at a MPW run of Fraunhofer HHI. Each FF includes two SOA-XGM switches, following the *"master-slave"* configuration [14].

Experimental Results

Fig. 2. (a)-(h) shows the synchronized time traces and spectra for the 2-bit optical AL operation at 10 Gb/s. In Fig. 2. (a) the stored bits of the optical FFs, at λ_1 and λ_2, of the two CAM cells corresponding to the logical *'0'* state, are presented. Fig. 2. (b) depicts the time traces of the Search-Line (SL) signal, prior being injected into the XOR gate of the optical CAM cells. The resulting traces of the CAM $cell_1$ and CAM $cell_2$ output are shown in Fig. 2. (c) and (d) along with their respective spectra. The two output signals are combined using an AWG producing a multi-level signal exhibiting three different power levels, that correspond to a different number of bit-level search miss, depicted in Fig. 2. (e) together with its respective spectrum. Fig. 2. (f) illustrates the output trace and spectrum of the ML signal after being propagated through the Encoding and Decoding circuit (En./Dec.), where a logical *'1'* appears only in the case of a "match" between the search and stored bit, while in every other case the result will be a logical *'0'*. Finally, the RAM Access traces and spectra at the output of the final MZI-AG, of the RAM $Cell_1$ and RAM $cell_2$, are illustrated In the Fig. 2. (g) and (h), respectively.

Fig. 3. depicts the spectra and time traces when a different AL table configuration is enforced, designated by the different λ_{10} value, targeting a RAM content of *'00'*. Fig. 3. (a) presents the spectrum at the RAM output, when both the CAM and RAM contents equal *'00'*, when the dominant wavelength is λ_6 and Fig. 3. (b) shows the spectrum when λ_8 is dominant. Fig. 3. (c) and (d) illustrate the respective traces for each dominant wavelength case.

Finally, the performance of the complete AL architecture was evaluated through BER measurements. Fig. 4 reveals the BER curves of the Back-to-Back (BtB), XOR outputs, ML and every RAM Access dominant wavelength, where in both cases the CAM content equals to *'00'* and the RAM content equals to *'00'* or *'01'*, respectively. The eye diagrams for every RAM dominant wavelength of the studied cases are also presented in Fig. 4., revealing an Extinction Ratio (ER) of around 5.8 dB for the case of RAM = *'00'* and 5 dB for RAM = *'01'*. Error-free operation was achieved for all experimental stages of the proposed architecture. Compared to BtB signal, the XOR operation for both CAM cells, features a power penalty of around 6 dB. The ML operation measurements indicate a power penalty of around 8 dB, while the memory access measurements feature a power penalty of around 9 dB, in comparison to the BtB measurements.

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