Accelerate Optical Network Modernization through Quantuminspired Digital Annealing

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Abstract In order to optimize migration plans for speedy network modernization, we developed an optimization problem formulation to utilize Fujitsu Digital Annealer. Compared to formulations tailored to commercial MIP solvers, our method found more optimal migration plans by up to 35%. ©2022 The Author(s)

Introduction

In recent years, telecom operators around the globe are struggling to manage their aging legacy SONET/SDH-based optical networks. For many operators, the installed SONET/SDH equipment has reached or long past its intended lifespan, resulting in more frequent equipment failures and higher risk of service outages. Meanwhile, these end-of-life infrastructures are also becoming increasingly costly to maintain, due to multiple challenges including lack of vendor support (e.g., replacement parts discontinued by the vendor, or sometimes the vendor itself is no longer in business), and lack of qualified personnel (e.g., hard to find technicians familiar with TDM technologies). For these reasons, an increasing number of operators have launched network modernization (NetMod) projects recently, with the aim of upgrading their legacy optical transport networks to modern platforms such as packetoptical employing OTN and circuit emulation.

In a NetMod project, prior to retiring a legacy network, all circuits carried by the legacy devices need to be migrated to a new network. Depending on the size, load and complexity of the legacy network, this migration process may take months or even years to complete [1]. Since a legacy device removal yields most prominent immediate benefits in terms of reduced OPEX (electricity, HVAC, backup battery, facility footprints, maintenance, etc.), reduced operational risk (service outages and losing customers), and increased revenue opportunity (e.g., vacated shelf space for new service offering), it is desirable to migrate circuits away from legacy devices in a most efficient way. Consequently, a well-designed circuit migration plan, which determines the network-wide circuit migration sequence, plays a crucial role in the speedy and cost-efficient NetMod execution [2,3].

A legacy device, such as a SONET/SDH

multiplexer or a Digital Cross-connect system (DCS), becomes 'zero-fill' after all its carried circuits have been migrated away. Such a zero-fill device can be safely removed from the network with no customer impact [4]. An optimized plan aims at achieving as many zero-fill devices as early as possible during circuit migration, thus accelerating the removal of legacy devices and launch of new network at the early stage of NetMod.

In a recent work addressing this problem [5], the authors formulate the circuit migration plan optimization problem as a Binary Quadratic Problem (BQP). BQPs are NP-hard in general. However, there are emerging technologies for solving BQPs, including quantum annealer by D-Wave Systems Inc. [6], CMOS annealers [7,8], and Coherent Ising Machines [9]. In [5], the authors leverage Fujitsu Digital Annealer (DA), which is a recent quantum annealing-inspired computer architecture capable of solving BQPs [10-12], and demonstrate that it can find feasible migration plans. However, circuit their formulation includes approximation, which leads to larger gaps between its solutions and optima in larger networks, thus less effective for practical usage.

In this paper, we present a new BQP formulation for DA without approximation, and compare its performance against formulations solved with a commercially available Mixed-Integer Programming (MIP) solver to demonstrate that our method finds more optimal migration plans by up to 35%.

Problem statement

As a metric for how early all devices in a legacy network become zero-fill overall, we introduce Time to Zero-fill (TTZ), which is the summation of devices in-service time across all circuit migration steps. For simplicity, we assume that one circuit is migrated per migration step, and one non-zero-



Tu1B.4

Fig. 1: An example of TTZ calculation for a network with 4 devices and 3 circuits (A-C).

fill device accrues one unit of in-service time in one migration step. Fig. 1 shows an example of TTZ calculation in a network with 4 devices and 3 circuits (A-C). With migration sequence of A-B-C, TTZ adds up as 4 (step 1/circuit A) + 4 (step 2/circuit B) + 0 (step 3/circuit C) = 8. On the other hand, with sequence of C-B-A, TTZ is only 3 + 2 + 0 = 5. Our goal is to find a circuit migration sequence that minimizes TTZ.

Proposed approach

We developed Integer Programming (IP) and High Order Binary Optimization (HOBO) formulations for this problem, which are solvable by Gurobi, one of the state-of-the-art commercially available MIP solvers. Then we also developed a BQP formulation to utilize DA.

As a basic formulation suitable for Gurobi, we developed the following IP formulation.

$$\min_{x_c, y_d} \sum_{d=1}^{N_D} y_d \tag{1a}$$

s.t.
$$y_d \ge x_c, \forall c \in P_d, \forall d = 1, ..., N_D$$
 (1b)
 $x_i \le x_c - 1 + N_c k_i, \forall i = 1, ..., N_d i > i$ (1c)

$$\begin{aligned} x_i &\leq x_j - 1 + N_C k_{i,j}, \forall i = 1, \dots, N_C, \forall j > i \\ x_i &\geq x_j + 1 - N_C + N_C k_{i,j}, \forall i = 1, \dots, N_C, \forall j > i \end{aligned} \tag{1c}$$

 N_C and N_D are constants denote the total number of circuits to be migrated and the total number of devices to be zero-fill respectively. Each circuit has an index $c \in \{1, ..., N_c\}$. Each device has an index $d \in \{1, ..., N_D\}$. P_d is a set of circuits carried on device d. If device 1 carries circuits 2 and 5 then $P_1 = \{2, 5\}$. $x_c \in \{0, ..., N_c - 1\}$ is an integer decision variable that denotes when (at which migration step) circuit c is migrated. $y_d \in$ $\{0, \dots, N_C - 1\}$ is an integer decision variable that denotes when device d becomes zero-fill. TTZ is calculated by $\sum_{d=1}^{N_D} y_d$ and Eq. (1a) is an objective function to minimize this. Eq. (1b) are constraints that a device becomes zero-fill only when all circuits carried on the device have been migrated. Eq. (1c) and (1d) are constraints that only one circuit is migrated in one step, which are generally called all-different constraint, simply expressed as $x_i \neq x_j$, $\forall i = 1, ..., N_C, \forall j > i$. Since Gurobi does not take all different constraint directly, we transformed this into Eq. (1c) and (1d) using a technique in [13] where k_{ij} is a binary

auxiliary variable.

We also developed the following basic HOBO formulation using binary decision variables instead of integer ones, with which Gurobi is expected to work well.

$$\min_{x_{c,t}, y_{d,t}} - \sum_{t=1}^{N_C} \sum_{d=1}^{N_D} y_{d,t}$$
(2a)

s.t.
$$y_{d,t} = \prod_{c \in P_d} x_{c,t}, \forall d = 1, ..., N_D, \forall t = 1, ..., N_C$$
 (2b)

$$x_{c,t} \le x_{c,t+1}, \forall c = 1, ..., N_C, \forall t = 1, ..., N_C - 1$$
 (2c)

$$\sum_{N_C}^{N_C} x_{c,t+1} - \sum_{N_c}^{N_C} x_{c,t} = 1, \forall t = 1, ..., N_C - 1$$
 (2d)

c=1 c=1 $x_{c,t}$ is a binary decision variable that denotes the status of circuit c at time t, which takes 0 if it is in service and 1 if it has been migrated. $y_{d,t}$ is a binary decision variable that denotes the status of device d at time t, which takes 0 if it is in service and 1 if it is zero-fill. TTZ is calculated by $N_{C} \times N_{D} - \sum_{t=1}^{N_{C}} \sum_{d=1}^{N_{S}} y_{d,t}$. Since we can ignore the constant part $N_C \times N_D$ while minimizing TTZ, we have Eq. (2a) as an objective function. Eq. (2b) are constraints that a device is zero-fill only when all circuits carried on the device have been migrated. Eq. (2c) are constraints that a circuit will never be recovered once it has been migrated. Eq. (2d) are constraints that only one circuit can be migrated at a time.

Gurobi can directly handle high order constraints in Eq. (2b), whereas DA is a BQP solver that processes linear or quadratic binary functions. Therefore, we transformed the HOBO formulation to a BQP formulation with the following techniques. First, we substituted Eq. (2b) into Eq. (2a) to have a high order objective function Eq. (3a).

$$\min_{x_{c,t}} - \sum_{t=1}^{N_C} \sum_{d=1}^{N_D} \prod_{c \in P_d} x_{c,t}$$
(3a)

In [14,15], the authors show that the high order objective function $\min_{x_i} - \prod_{i=1}^{N} x_i$ is equivalent to the quadratic objective function $\min_{x_i} v(\sum_{i=1}^{N} 1 - \sum_{i=1}^{N} x_i - 1)$. v is a binary auxiliary variable to ensure that both functions take the same value for all possible combinations of x_i . By introducing this transformation, we have the following BQP

objective function.

$$\min_{x_{c,t}} \sum_{t=1}^{N_C} \sum_{d=1}^{N_D} v_{d,t} \left(\sum_{c \in P_d} 1 - \sum_{c \in P_d} x_{c,t} - 1 \right)$$
(4a)

Tu1B.4

DA has a feature dedicated to the acceleration of solving problems with 1-hot constraints, where a single variable takes 1 and the others take 0 in a group of binary decision variables. To take advantage of this feature, we introduced a variable $z_{c,t}$ that denotes the timing of migrating circuit c, which takes 1 only if the circuit c is migrated at migration step t. By using $z_{c,t}$ instead of $x_{c,t}$, we can replace constraints Eq. (2c) and (2d) with equivalent 1-hot constraints. We also transformed the objective function Eq. (4a) with $x_{c,t} = \sum_{r=1}^{r=t} z_{c,r}$ to have the following final BQP formulation suitable for DA.

$$\min_{z_{c,r}} \sum_{t=1}^{N_C} \sum_{d=1}^{N_D} v_{d,t} \left(\sum_{c \in P_d} 1 - \sum_{c \in P_d} \sum_{r=1}^{r=t} z_{c,r} - 1 \right)$$
(5a)

s.t.
$$\sum_{N_c}^{N_c} z_{c,t} = 1, \forall c = 1, ..., N_c$$
 (5b)

$$\sum_{c=1}^{N_{c}} z_{c,t} = 1, \forall t = 1, \dots, N_{c}$$
 (5c)

Evaluation

We compared IP and HOBO solved with Gurobi V9.1.1 using 32 cores on Intel (R) Xeon (R) Platinum 8176 CPU@2.10GHz, and BQP solved with 3rd generation DA [12] in an environment exclusive for research purpose. The solutions were evaluated in terms of TTZ and computation time. We used three topologies (France, India, Pioro) from SNDlib datasets [16] as legacy networks, which have 25, 35, and 40 nodes respectively. We assumed that each node corresponds to a legacy device, and used the shortest paths consist of nodes between pairs of source and destination nodes in the datasets as circuits targeted for migration.

Tab. 1 shows TTZ of circuit migration solutions for different number of circuits minimized by each method under 1800 s of

	Circuit	BQP	ново	IP
France	80	986	986	987
	100	1279	1279	1286
	200	2995 (-5%)	3144	3730
	290	4987 (-20%)	6209	6963
India	80	1414	1414	1425
	100	1873	1873	1898
	200	3922 (-8%)	4264	5830
	290	6043 (-35%)	9368	9356
Pioro	80	1635	1632	1632
	100	2057	2055	2075
	200	4510 (-16%)	5371	6034
	290	7028 (-35%)	10933	10865

Tab. 1: TTZ under 1800 seconds.



Fig. 2: Time development of TTZ for France (290 circuits).



Fig. 3: Time development of TTZ for Pioro (290 circuits).

computation time. The numbers shown in parentheses are the ratios of reduction to the second-best solutions. The three methods are almost comparable for 100 circuits and below, while BQP (DA) is superior to others for 200 and 290 circuits and reduces TTZ by 20 to 35 % than the second-best solutions for 290 circuits. We only evaluated up to 290 circuits and up to 1800 s due to current limitation of DA configuration in our environment, which can be scaled up with configuration change.

Fig. 2 and 3 show time development of TTZ for France and Pioro with 290 circuits. For both cases, BQP (DA) is much faster in computation time than the second-best HOBO to reach equivalent TTZ: more than 20 times faster for both cases. India results exhibit similar tendency and are not shown due to space limit.

Conclusions

In this paper, we developed a new BQP formulation to utilize Fujitsu Digital Annealer for generating optimized NetMod solutions. Compared to IP and HOBO formulations solved by a commercial MIP solver, the BQP/Digital Annealer approach achieves up to 35% solution efficiency improvement and over 20x execution speed for networks with up to 290 circuits. These results suggest the effectiveness of the new approach in contributing to an accelerated worldwide progress of optical network modernization.

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Tu1B.4

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