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System Performance Assessment of an Optical Wireless Data Center Network based on Photonic Integrated Multicast Switch

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Abstract *We propose an OW-DCN using a nanoseconds photonic integrated SOA based multicast switch chip to realize fast optical packet switching. System experiments with a fabricated 4×2 switch chip in a 4×4 rack OW-DCN show a WDM multicast switch operation at 50Gb/s with <1.5dB power penalty. ©2022 The Author(s)*

Introduction

Driven by the ever-increasing 5G applications and cloud computing paradigm, heterogeneous traffic volumes have to be handled by a data center network (DCN) [1]. Conventional multiple-layer DCNs, which are based on electrical switches and fiber connections, suffer from significant problems of low bandwidth, high latency, poor scalability, low flexibility, high cost, and high energy consumption. These aforementioned problems require architectural and technological innovations of DCN solutions to satisfy the scalable growth in traffic volumes. The optical wireless DCN (OW-DCN) employing optical switch technology and optical wireless communication could be an attractive solution. The transparent optical networks with fast optical switching technology eliminate the O/E/O conversion, resulting in low power consumption with high data rates [2]. At the same time, wireless technology makes it possible to move towards ultra-high data rates and high flexibility with a wide unlicensed spectrum range, negligible waveguide dispersion and attenuation [3], as well as plug-and-play wireless modules.

Several technologies have been applied to propose an OW-DCN, such as MEMS [4], digital micro-mirror devices [5], switchable mirrors [6], photonic integrated circuits [7], and mechanically steerable links [8]. However, most of these approaches do not take into account some major issues, such as the switching speed, control complexity, component size, and power consumption, which leads to large latency, slow reconfigurability, poor scalability, and low efficiency.

In this paper, we propose and experimentally demonstrate a photonic integrated multicast switch (PIC-MCS) to realize a nanosecond tunable transmitter for optical packet switching in an OW-DCN. A 4×2 PIC-MCS chip has been designed and fabricated. The system performance has been verified within a 4×4 rack DCN built with the chip and a 4×4 AWGR. Bandwidth allocation and WDM multicast transmission with 50Gb/s NRZ-OOK signals have been verified, which shows less than 1.5 dB power penalty with respect to the back-to-ack transmissions.

System Operation and PIC-MCS Chip

The general architecture of the OW-DCN based on TORs with tunable TRXs using discrete components and passive arrayed waveguide grating router (AWGR) is shown in Fig. 1(a). This architecture has been already demonstrated in [9] using discrete SOAs to implement the fast tunable TRXs. It consists of two parallel intra- and inter-cluster networks. An intra-cluster AWGR-based switch (IAS) interconnects N ToRs within one cluster through the intra-cluster optical wireless links. The inter-cluster network, consisting of N AWGR-based switches (EAS), is

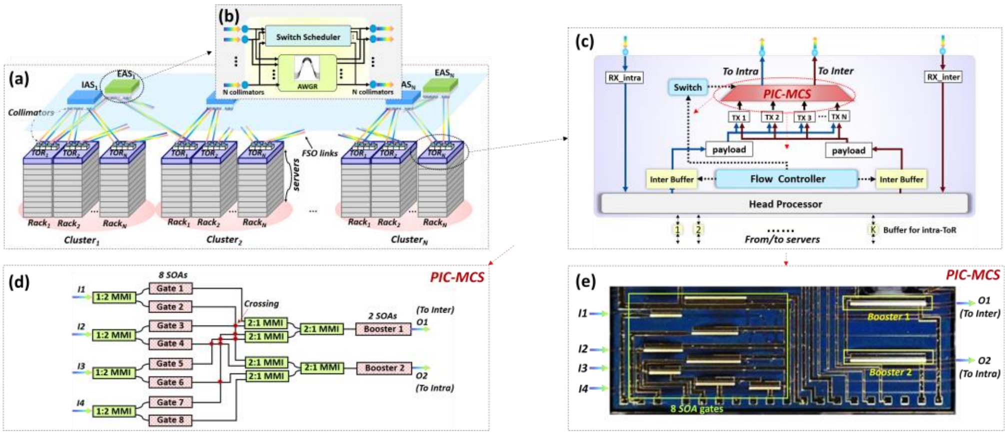

Fig. 1: (a) A schematic diagram of the OW-DCN; (b) The functional blocks of the AWGR-based optical switch; (c) The functional blocks of PIC-MCS based ToR switch; (d) The schematic of the 4 × 2 MCS chip; (e) The microscope image of the 4 × 2 MCS chip.

used for interconnecting the ToRs of different clusters via the inter-cluster optical wireless links, namely, the *i*-th EAS interconnect the *i*-th (1≤ *I* ≤ *N*) ToR of each cluster. The optical wireless links are established by collimators placed on ToRs and optical switches (EAS and IAS). The fast optical packets switching between the *N*×*N* optical ToRs is achieved by employing fast tunable transmitters at the ToR side (see Fig. 1(c)) and passive *N*×*N* AWGRs at the EAS or IAS side, see functional block in Fig. 1(b). Tab. 1 shows a corresponding wavelength routing map for a *N*×*N* AWGR to interconnect *N* ToRs within an intra- or inter-cluster networks. The center wavelengths of the *N* TXs are chosen accordingly as λ1 to λ*N* for matching the wavelength routing map of the AWGR. The fast tunable transmitters at the ToRs are constructed by an *N*×*2* PIC-MCS, capable of forwarding the data streams from the *N* transceivers (TX) seamless to the intra- or/and inter-clusters switches according to the required capacity allocation. The *N*×*2* PIC-MCS, which consists of *N*+2 on-chip SOAs, enables parallel optical packet-level switch processing between the four TX according to the switching control signals from the FPGA-based ToRs. It should be noticed that the PIC-MCS gives multiple advantages to this OW-DCN. It realizes dynamic wavelength selection between the TXs, as well as achieving a nanosecond timescale optical packet switch. Moreover, the TXs are shared between the intra- and inter- cluster with the help of this single chip, which reduces the footprint and cost of the system and further realizes on-demand bandwidth allocation between intra- and inter- cluster transmission for dynamically adapting to the rapid traffic changes.

The schematic and the microscope image of the 4×2 PIC-MCS designed and fabricated on the InP platform are shown in Fig. 1(d) and (e). Signals from four input ports can be switched and broadcasted to any of the two output ports simultaneously. Specifically, the optical signal coming from four input ports are firstly spitted by four 1x2 multimode interferometers (MMI) and fed into eight quantum well active SOA gates. The outputs of the SOA gates are connected to two 4×1 combiners, which are based on cascaded 1×2 MMIs. Two 1000um SOAs are employed as amplifiers to compensate for the on-chip splitting losses and fiber-to-chip coupling losses. Therefore, the optical signals are guided to two output ports (intra- and inter- cluster output ports) to reach the EAS and IAS. Turning on and off the 8 SOA gates determines which signals are sent (multicasted) to the optical switch (EAS or IAS) or which signals are blocked. Therefore, one photonic integrated switch chip can select one or more optical channels and forward the signals to both the EAS and IAS in an independent and parallel way. Moreover, the switching time of the chip is independent of the port count and equal to the switching time of a single SOA.

Tab. 1: Wavelength routing map of a *N*×*N* AWGR between *N* ToRs within an intra-/inter-cluster network.

AWGR	O1 (ToR1)	O2 (ToR2)	O3 (ToR3)	…	ON (ToRN)
I1 (ToR1)	λ0	λ1	λ2	…	λN
I2 (ToR2)	λ1	λ2	λ3	…	λ0
. . .	. . .	. . .	. . .	. . .	. . .
IN (ToRN)	λN	λ0	λ1	…	λ(N-1)

Experimental Set-up and Results

In order to evaluate the performance of the fabricated 4×2 PIC-MCS chip under the proposed OW-DCN system, an experimental setup is built with the chip and a 4×4 AWGR as one cluster with 4×4 racks OW-DCN. Different transmission scenarios have been assessed, namely single-channel transmission, simultaneously intra-/ inter- cluster transmission, and multicast transmission. The setup shown in Fig. 2 is used where four optical signals from the transmitter are switched by the chip for inter- or intra- cluster transmission as the tunable transmitter. While the 4×4 AWGR worked as the EAS or IAS route the switched optical signals to the destination ToRs. Two pair of collimators (Thorlabs TC18FC-1550) constructs the two bi-directional optical wireless links for the interconnection between the AWGR and the Tx-/ RX- ToRs. Specifically, according to the routing map of the AWGR, four lasers at 1550.94nm (λ_1), 1546.14nm (λ_2), 1547.75nm (λ_3), and 1549.34nm (λ_4) and a 50 Gb/s NRZ-OOK optical Mach-Zehnder modulators (MZM) are employed as optical transmitters for ToR_{14} to assess the transmission to other intra- and inter-cluster ToRs within the 4×4 rakes DCN. A de-multiplexer is used to separate and decorrelate the four optical signals. The optical power of the four optical signals were around -3 dBm/channel. The chip is temperature-controlled at 20ºC using a water cooler, and lensed fibers are utilized to couple light in and out of the chip. The electrodes of the on-chip SOAs are routed through on-chip metal tracks and then wire-bonded to neighbouring PCBs to enable the switch control and amplification. The gate and booster SOAs were biased with currents of 30 and 42 mA,

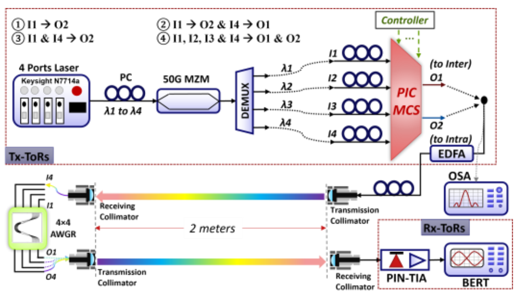

Fig. 2: The experimental setup to assess the performance of the 4×2 PIC-MCS within a 4×4 racks DCN.

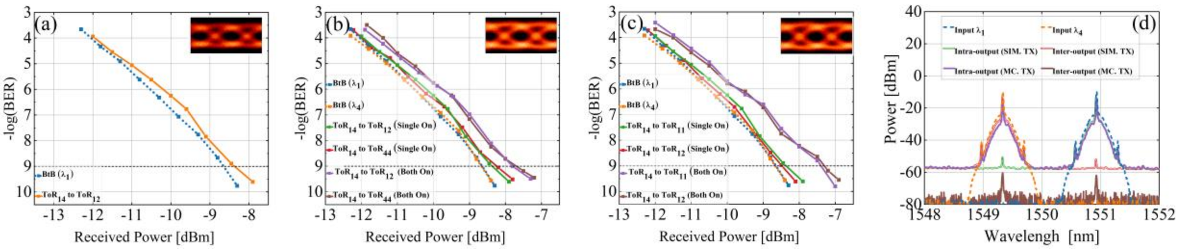

Fig. 3: (a) Eye diagram and BER curves of the single-channel transmission; (b) Eye diagram and BER curves of the intra- & inter- cluster transmission; (c) Eye diagram and BER curves of the multicast transmission; (d) Optical spectra from O1 and O2 of the chip.

respectively. Polarization controllers have been employed at the inputs of the chip and after each laser source.

First, the single-channel transmission was evaluated by injecting the optical signal λ_1 into the input port 1 (I1) and switched out from output port 2 (O2). The SOA gate 2 and the SOA booster 2 are enabled. Around -6.5 dBm output power is observed at O2. Considering an average of 6 dB/facet fiber-to-chip coupling losses and 9 dB splitting losses from 3 cascaded MMIs, it was estimated that the on-chip losses were on the range of 21 dB. Thus, around 17.5 dB on-chip gain is achieved. After that, the modulated signal λ_1 is sent to the AWGR-based free-space system and measured by a bit error rate tester (BERT) at the Rx-ToR. Clear eye openings and error-free operation with a power penalty of less than 0.5 dB are obtained, as shown in Fig. 3(a). Additionally, the parallel intra-/inter-cluster and multicast transmission have been verified. Two optical signals (λ_1 and λ_4) are injected into I1 and I4. Simultaneously intra- and inter-cluster transmission is performed by switching λ_1 to O2 for intra-cluster transmission with ToR_{12}, while λ_4 is switched to O1 for inter-cluster transmission with ToR_{44} in parallel. As for the multicast transmission, both of the optical signals (λ_1 and λ_4) are switched to O2 to reach the two intra-cluster ToRs (ToR_{11} and ToR_{12}) simultaneously. Measurements are carried out for (i) both λ_1 and λ_4 optical data signals are switched on, (ii) only one optical data signal is present, and the other is absent. The BER curves of simultaneously intra-/inter cluster and multicast transmission are shown in 3(b) and (c), respectively. The power penalty is around 1dB and 1.5dB at BER=10^{-9} for the simultaneously intra-/inter- cluster transmission and the multicast transmission, respectively. Besides, clear open-eye diagrams of the switched channels (λ_1) are observed in the presence of λ_4 at BER=10^{-9}. Moreover, the spectra out from O1 and O2 are captured, as depicted in Fig. 3(d). By analyzing the spectral contents of simultaneously intra-/inter-cluster transmission, around 40 dB contrast ratio of the chip is measured for the selected channels with respect to the blocked ones. Meanwhile, since the booster SOA for inter-cluster transmission is off for the multicast transmission, over a 50 dB contrast ratio is observed. Lastly, the capability of dynamic bandwidth allocation between the intra- and inter-cluster is realized by feeding the four 50Gb/s optical signals into the four input ports parallelly and switching on/off the corresponding SOA gates. The received spectra at the chip's two output ports (intra- and inter-cluster) are shown in Fig. 4. As we can see, there are three different transmission scenarios. λ_2 and λ_4 are dynamically shared for intra-cluster transmission (ToR_{14} to ToR_{11} and ToR_{13}) and inter-cluster transmission (ToR_{14} to ToR_{24} and ToR_{44}), which shows the potential of the dynamic quality of service provisions of the chip for improving network utilization efficiency. Thus, the dynamic bandwidth allocation and successful WDM multicast transmission for intra-/inter-cluster networks have been demonstrated, which validates the chip's switching operation and confirms the system's dynamic switch capability.

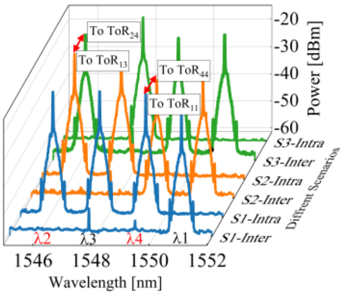

Fig. 4: Bandwidth allocation between intra-/ inter- cluster.

Conclusion

We have fabricated a photonic integrated MCS as one of the main building blocks for an OW-DCN. The SOA-based 4×2 PIC-MCS can provide fast switching and amplification for the optical packet signals. The chip has been employed with a 4×4 port AWGR to validate the link performance of a 4×4 rack OW-DCN. Error-free operation at 50 Gb/s with <1.5 dB power penalty is achieved both for a single-channel, simultaneously intra-/ inter-cluster transmission, and multi-channel transmission. The dynamic bandwidth allocation capability further confirms the utilization efficiency of the chip. This single PIC-MCS chip not only realizes dynamic wavelength selection between the TXs as a tunable transmitter but also achieves a nanosecond timescale optical packet switch. The possibility of integrating chips for all-optical switching is highly attractive for the next generation DCN.

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