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All-Optical Dual-Polarization MIMO Processor based on Integrated Optical Unitary Converter

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Abstract *A 6-port optical unitary converter circuit with polarization-splitter-rotators is realized on a compact silicon photonic chip. All-optical MIMO demultiplexing of 300-Gbps 3-mode DP-QPSK signal is demonstrated with an energy consumption of around 1.5 pJ/bit. ©2022 The Author(s)*

1. Introduction

Space-division multiplexing (SDM) technology plays a crucial role in supporting the next-generation Peta-bit/s-class optical communication systems [1,2]. Due to the inevitable inter-modal coupling during the transmission through a multi-mode fibre (MMF) or a multi-core fibre (MCF), multi-input multi-output (MIMO) process is required at the receiver to retrieve the signals. While this is typically performed through the electronic digital signal processing (DSP) after coherent detection [1-3], its complexity and power consumption scale super-linearly as the number of modes increases [4].

To cope with this problem, all-optical MIMO has been considered [5-7]. As shown in Fig. 1, an all-optical MIMO circuit at the receiver can unscramble mixed multi-mode optical signals with nominal power consumption, which is transparent to the signal baudrate and the modulation format. The previous experimental demonstrations of all-optical MIMO, however, were limited to either a single-polarization operation without using an actual MMF link [6] or with a single-output-channel device that could only demultiplex multiple channels sequentially [7].

In this paper, we demonstrate simultaneous all-optical MIMO demultiplexing of dual-polarization (DP) 3-mode-multiplexed signals by a compact silicon photonic chip for the first time. The device consists of polarization-splitter-rotators (PSRs) attached at the three input ports, followed by a 6-port arbitrary optical unitary converter (OUC) circuit to unscramble both the spatial and polarization modes in a reconfigurable manner. Using the fabricated device, we experimentally demonstrate demultiplexing of 3-mode 25-Gbaud DP quadrature-phase-shift-keying (QPSK) signals (300 Gbps in total) with a bit error ratio (BER) below the soft-decision forward error correction (SD-FEC) threshold. The energy cost required at the all-optical MIMO processor is derived to be less than 1.5 pJ/bit, which should further decrease at a higher signal rate.

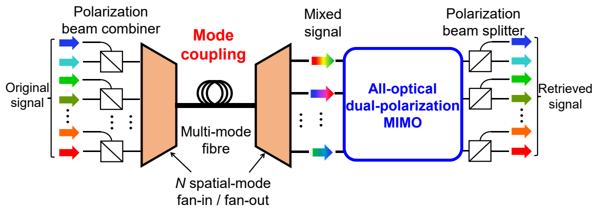

Fig. 1: Schematic of all-optical MIMO system using reconfigurable OUC.

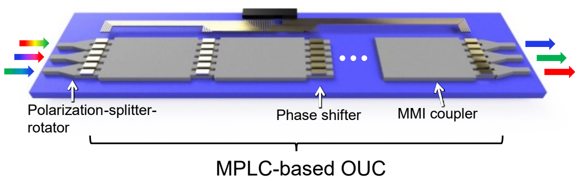

Fig. 2: Schematic of the all-optical MIMO processor demonstrated in this work. It consists of PSR section and OUC section. The OUC part consists of cascaded MMI couplers and phase shifter arrays

2. Design and fabrication of all-optical MIMO processor chip

The schematic of the 3-mode DP all-optical MIMO processor chip is shown in Fig. 2. The three DP signals, which are connected from the fan-out device (e.g., photonic lantern) as shown in Fig. 1, are first polarization-demultiplexed by the integrated PSR attached at each port. The output ports of the PSRs are then guided to a 6-port arbitrary OUC circuit based on the multi-plane light conversion (MPLC), where appropriate linear transformation is applied to compensate for all the coupling effects among the spatial/polarization modes.

The PSR is based on the adiabatic polarization rotator to convert the TM_0 mode into TE_1 mode while maintaining the TE_0 mode [8]. Then, the linear superpositions of TE_0 and TE_1 modes are split by a mode-independent Y-splitter designed by the particle swarm optimization [9]. As a result, the input DP signal

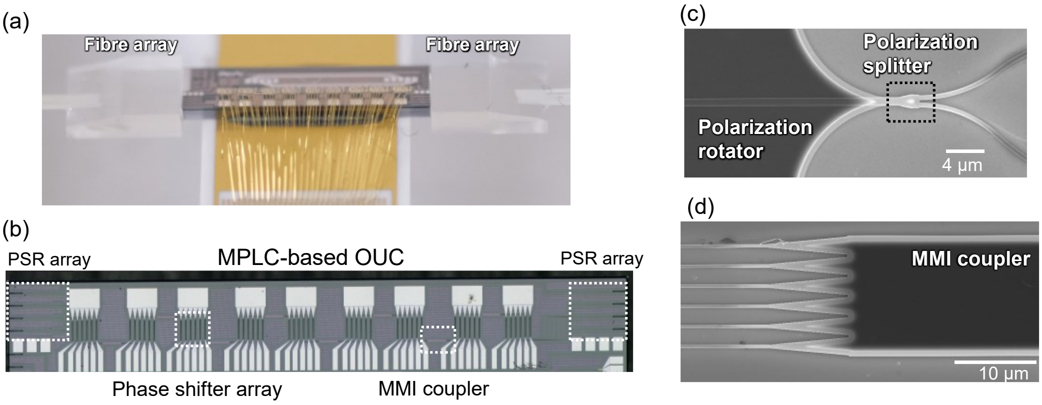

Fig. 3: (a) Image of the mounted chip and (b) microscope image. All electrodes are wire-bonded and fiber arrays are connected. (c)(d) The SEM images of (c) polarization rotator and splitter, and (d) MMI coupler

with complex amplitudes of a_{TE0} and a_{TM0} is split to two output ports with amplitudes of $1/\sqrt{2}\,(a_{\mathrm{TE0}} + a_{\mathrm{TM0}})$ and $1/\sqrt{2}(a_{\mathrm{TE0}} - a_{\mathrm{TM0}})$. We should note that unlike a typical PSR [8], it is not necessary to split a_{TE0} and a_{TM0} in our device, since any linear coupling can be removed anyway at the OUC section.

The OUC section is based on the concept of MPLC, where multimode interference (MMI) couplers and phase shifter arrays are cascaded [10]. The transfer matrix $\mathbf{U}$ of an MPLC-based OUC is written as

$$\mathbf{U} = \mathbf{\Phi}_L \bullet \mathbf{T} \bullet \mathbf{\Phi}_{L-1} \bullet \mathbf{T} \bullet\bullet\bullet\, \mathbf{T} \bullet \mathbf{\Phi}_0, \qquad (1)$$

where $\mathbf{T}$ and $\mathbf{\Phi}_i$ $(i = 0,1,\cdots L)$ are the transfer matrices of a MMI coupler and a phase shifter array, respectively. Each $\mathbf{\Phi}_i$ includes N (when i = 0) or N-1 (when $i \neq 0$) phase shifters so that $N+L\times(N-1)$ phase shifters in total are employed. It is shown that if $L \geq N$, this circuit can realize arbitrary unitary conversion by appropriately setting the phase shifters [10-14]. In this work, we set L = 8 and N = 6.

Figure 3 shows the photograph and the scanning-electron microscope (SEM) images of the device fabricated on a silicon-on-insulator (SOI) platform with a 210-nm-thick silicon and 3-μm buried oxide (BOX) layers. The device consists of PSR arrays, 9 stages of 200-μm-long thermo-optic (TO) phase shifter array with TiN heaters, and 8 stages of 6×6 MMI couplers. The width and the length of an MMI coupler are 15 μm and 268 μm, respectively. The total number of phase shifters is 54. While PSRs are not necessary at the output, they are included in this work to reduce the number of ports that need to the coupled to the output fibre array.

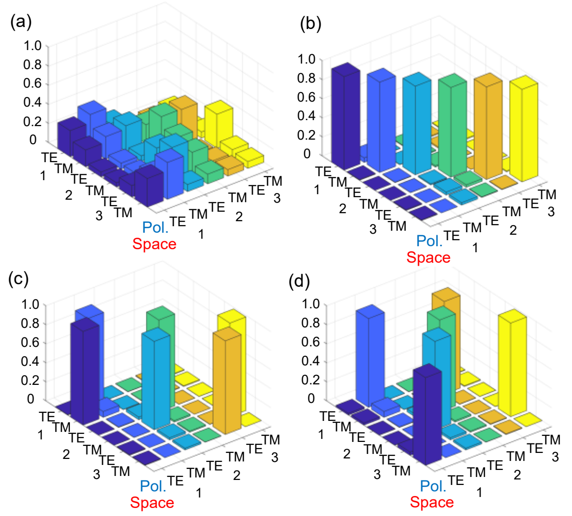

Fig. 4: Measured optical transmission from 6 input modes (3 spatial × 2 polarization) to 6 output modes (a) before optimization and (b)-(d) after optimization. In all cases, the crosstalk is suppressed to be less than -10 dB.

From preliminary measurements, we derive the coupling loss between a fibre array and the chip to be ~3.5 dB/facet, the insertion loss of a 6×6 MMI coupler to be ~1.5 dB, and V_π of the phase shifter as 3.1 V.

3. All-optical MIMO experiment

First, we confirmed the performance of reconfigurable OUC operation using a similar setup as described in [14]. Figure 4 shows the measured transmission matrices before (Fig. 4 (a)) and after (Fig. 4(b)-(d)) optimization at 1550 nm wavelength. In all cases, the crosstalk is suppressed to be less than -10 dB.

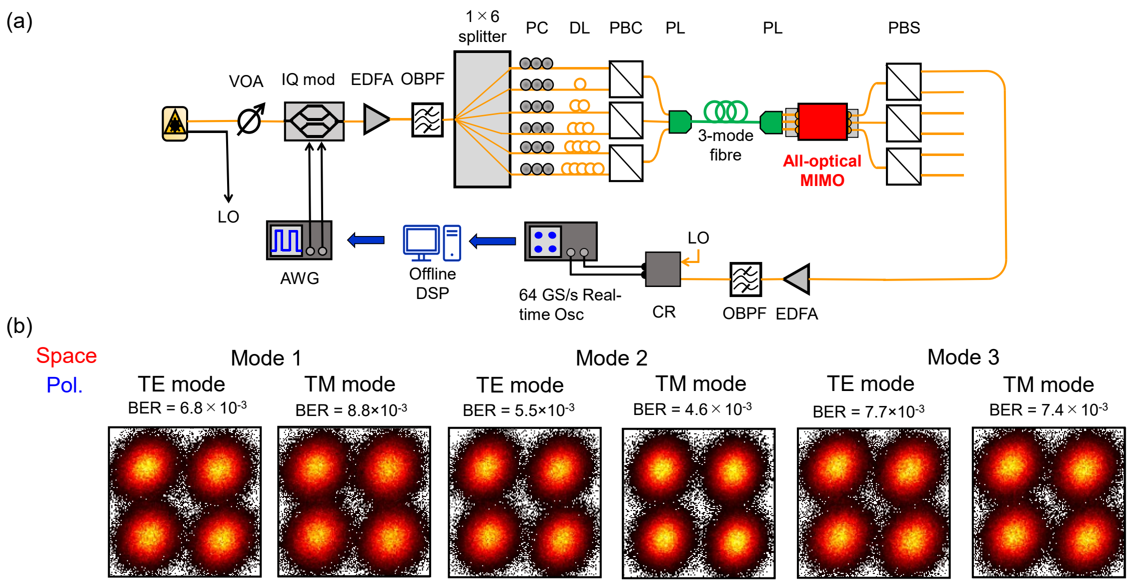

Fig. 5: (a) Experimental setup for all-optical MIMO process with mode-multiplexed DP-QPSK signal. TLS: tunable laser source, VOA: variable optical attenuator, EDFA: erbium-doped fiber amplifier, OBPF: optical band pass filter, PC: polarization controller, DL: delay line, PBC: polarization beam combiner, PL: photonic lantern, FMF: few-mode fiber, PBS: polarization beam splitter, CR: coherent receiver, AWG: arbitrary wave generator. (b) Constellation of retrieved 50-Gbps QPSK signals after optical MIMO process and offline DSP.

Then, all-optical MIMO experiments were performed using the setup shown in Fig. 5(a). A $LiNbO_3$ in-phase and quadrature (IQ) modulator was driven by a two-channel arbitrary waveform generator (AWG) to generate a 25-Gbaud QPSK signal. The signal was split into six branches, decorrelated by fibre delay lines, and combined by three polarization beam combiners (PBCs) and a photonic lantern (PL). For the proof-of-concept demonstration, we employed a 1-m-long 3-mode MMF in this work. At the output of the MMF, the signal was split by another PL and input to the all-optical MIMO processor. The output signals from the chip were separated by polarization beam splitters (PBSs) to receive each spatial/polarization mode by a coherent receiver (CR). Through offline DSP, the measured signals were down-sampled and then equalized by half-symbol-spaced adaptive finite-impulse-response (FIR) filters. We employed the decision-driven least-mean-square (DD-LMS) algorithm, which was the same procedure as used in [15]. We should note that the MIMO process was fully performed in the optical domain, and not by the DSP.

Figure 5 (b) shows the constellation diagrams of 50-Gbps QPSK signals for all 3 spatial modes and both polarizations. In all cases, we obtain BERs below the 20% SD-FEC threshold. The residual penalty is partially attributed to the imperfect mode demultiplexing inside the OUC section as shown in Fig. 4. We thus expect it could be improved by applying more efficient optimization algorithm instead of the simulated annealing. The total power consumption at all 54 phase shifters is derived to be around 450 mW. This corresponds to an energy cost of around 1.5 pJ/bit for the 300-Gbps signal. As a unique advantage of the all-optical MIMO, the power consumption is independent on the bitrate. This implies that the energy cost (J/bit) would decrease inversely as we increase the bitrate.

Conclusions

We have experimentally demonstrated all-optical MIMO demultiplexing of 3-mode DP coherent signals for the first time. Using a silicon photonic chip, composed of adiabatic PSR arrays and the MPLC-based 6-port OUC circuit, we successfully achieved demultiplexing of mode/polarization-scrambled 300-Gbps QPSK signal with the BER below the 20% SD-FEC threshold. Owing to the ultralow energy consumption of around 1.5 pJ/bit, which would further decrease as we increase the baudrate, the demonstrated device should be attractive in realizing the future cost- and power-efficient SDM transmission systems.

Acknowledgements

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