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Spiking Neural Network Equalization on Neuromorphic Hardware for IM/DD Optical Communication

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Abstract *A spiking neural network (SNN) nonlinear equalizer model is implemented on the mixed-signal neuromorphic hardware system BrainScaleS-2 and evaluated for an IM/DD link. The BER 2e-3 is achieved with a hardware penalty less than* $1\,\mathrm{dB}$*, outperforming numeric linear equalization. ©2022 The Author(s)*

Introduction

Cloud services cause an exponentially growing traffic in data centers. This requires optical transceivers to operate at lower power and lower cost. Because digital signal processing (DSP) has high power consumption, recent research envisions replacing the DSP in part with an analog frontend with lower power consumption. One approach is photonic neuromorphic computing [1], which has been proposed, e.g., for chromatic dispersion (CD) compensation and nonlinear equalization in short-reach optical transmission [2, 3]. A second approach is analog electronic neuromorphic computing, which implements spiking neural networks (SNNs) [4] in analog hardware [5], adopting the brain's unique power efficiency by imitating the basic functioning of the human brain. Recently, in-the-loop (ITL) training of SNNs on analog hardware [6] has shown promising results by achieving state-of-the-art performance in inference tasks [7]. Although photonics is operating faster than electronic hardware, the latter scales better and can therefore achieve higher throughput by parallelization. Electronic hardware is therefore tailored for low power signal processing.

In Arnold *et al.* [8], we design and evaluate an SNN equalizer in a software simulation for the detection of a pulse amplitude modulation 4-level (PAM4) signal for an intensity-modulation / direct-detection (IM/DD) link, impaired by CD and additive white Gaussian noise (AWGN). The results show that in principle, SNNs can perform as well as nonlinear artificial neural network (ANN) equalizers, outperforming linear equalizers.

However, to assess the applicability of SNNs for equalization in practical systems, evaluation in hardware is essential.

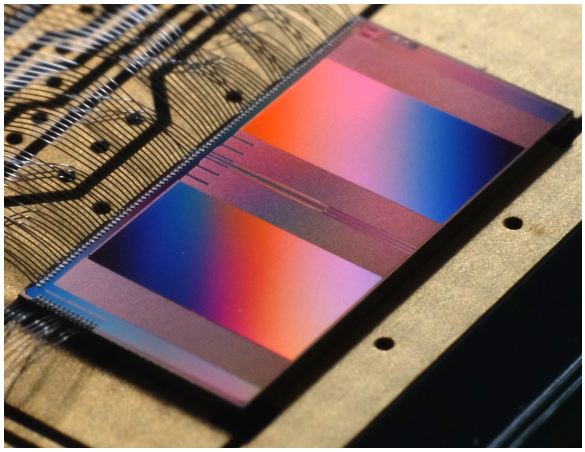


Fig. 1: A BrainScaleS-2 application-specific integrated circuit (ASIC) bonded to a carrier board. The chip is about $4\,\mathrm{mm} \times 8\,\mathrm{mm}$ in size.

In this work, we design and implement SNNs for joint equalization and demapping on the mixed-signal neuromorphic BrainScaleS-2 (BSS-2) system [5] displayed in Fig. 1. We showcase that an SNN equalizer/demapper trained on the analog substrate efficiently detects a PAM4 signal of an IM/DD link enabling a $200\,\mathrm{Gbit/s}$ transmission with $12\,\%$ overhead hard-decision forward error correction (FEC), outperforming numeric linear equalization. Furthermore, we compare the bit error rate (BER) achieved on BSS-2 to ANN and SNN equalizers simulated in software.

Simulated IM/DD Link

As an application scenario, we simulate a $200\,\mathrm{Gb/s}$ IM/DD transmission over $4\,\mathrm{km}$ in the O-band. We assume a $12\,\%$ overhead FEC with a BER threshold 2×10^{-3} and a corresponding baudrate of $112\,\mathrm{GBd}$. Our model is displayed in Fig. 2A and parameters are summarized in Fig. 2C. A bit sequence $([B_1 B_2]^t)_{t\in\mathbb{N}}$ is mapped

to a PAM4 signal, which is upsampled and filtered with a root-raised-cosine (RRC), after which a positive bias is added. Transmission through the fiber is then simulated by applying CD. At the receiver, a photodiode (PD) squares the signal and AWGN is added. The signal is then RRC filtered and downsampled. The resulting sequence $(y^t)_{t\in\mathbb{N}}$ is equalized and demapped, resulting in the bit decisions $([\hat{B}_1\hat{B}_2]^t)_{t\in\mathbb{N}}$.

Spiking Neural Network Equalizer/Demapper

Besides minor adaptations, we consider an SNN equalizer/demapper as described in our recent work [8] and which we summarize next. Our SNN architecture has one hidden layer of 40 leaky-integrate and fire (LIF) neurons [4, Sec. 1.3], projecting spike events onto four leaky-integrate (LI) readout neurons [4, Sec. 1.3]. The membrane potential v_j of LIF neurons is described by the ordinary differential equation (ODE)

$$\tau_{\mathsf{m}}\dot{v}_j(\rho) = -\left(v_j(\rho) - v_{\mathsf{l}}\right) + I_j(\rho), \qquad (1)$$

with v_{l} the leak potential, τ_{m} the membrane time constant and I_j the current onto neuron j caused by pre-synaptic events. As v_j exceeds a threshold ϑ, neuron j sends out a spike at time ρ_j^s and is set to a reset potential v_{r}. The current I_j onto neuron j is given by the exponentially filtered pre-synaptic spike train,

$$I_j(\rho) = \sum_i \sum_{\{\rho_i^s\}} W_{ji}\Theta\left(\rho - \rho_i^s\right)\exp\left(\frac{\rho_i^s - \rho}{\tau_{\mathsf{syn}}}\right) \qquad (2)$$

with synaptic time constant τ_{syn} and ρ_i^s the spike times of the pre-synaptic neurons $\{i\}_{i=1}^{<n^{\mathsf{i}}}$. The membrane potential v_k of LI neurons is subject to the same dynamics, without the ability to spike. That is, current I_k, caused by spikes of the hidden LIF neurons $\{j\}_{j=0}^{<n^{\mathsf{h}}}$, is integrated onto the LI membranes.

For demapping a transmitted sample y^t, we assign each sample $y_l^t \in \mathcal{C} = \left[y^{t-\lfloor n_{\mathsf{tap}}/2\rfloor}, y^{t+\lfloor n_{\mathsf{tap}}/2\rfloor}\right]$ (n_{tap} odd and $l \in \mathbb{N}_0^{<n_{\mathsf{tap}}}$ indexing $\mathcal{C}$) $n^{\mathsf{i,\,tap}} = 10$ input neurons, emitting spikes at times ρ_i^s with $i = n^{\mathsf{i,\,tap}}\cdot l + h$ and $h \in \mathbb{N}_0^{<n^{\mathsf{i,\,tap}}}$. Note that the time ρ is the time axis within the time frame between two samples at time steps t and $t+1$. The spike times ρ_i^s are given by a linear scaling of the distances of y_l^t to reference points χ_h. Finally, y^t is labeled with the class $k \in \{0,1,2,3\}$ for which the corresponding readout neuron has the maximum membrane value over time, i.e. $\mathrm{argmax}_k \max_\rho v_k(\rho)$. Thus, the network's objective is to learn to adjust the hidden neurons such that their spikes tune the membrane potentials of the output neurons meaningfully.

Because of the non-differentiable output of spiking LIF neurons, we use surrogate gradients (SuperSpike [9]) in conjunction with back-propagation through time (BPTT) to train our SNNs. Weights are optimized with the Adam optimizer [10].

BrainScaleS-2 System

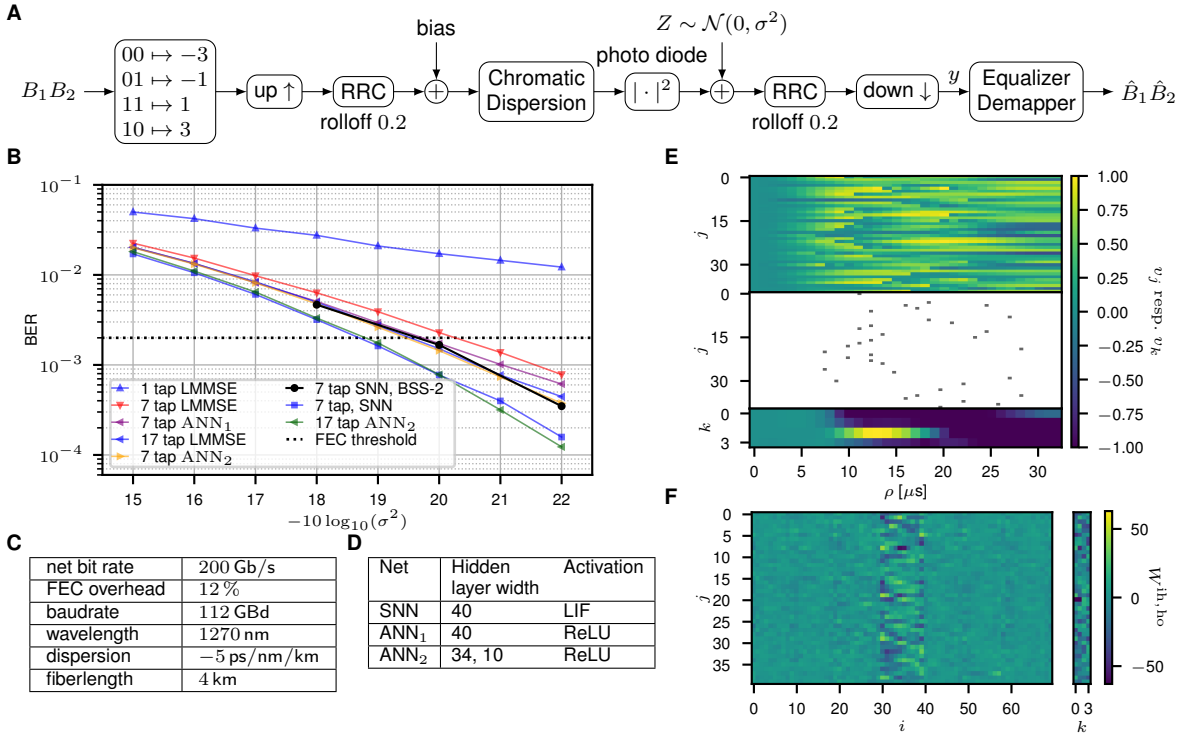
We deploy our SNN equalizer/demapper on the accelerated mixed-signal neuromorphic BSS-2 system, developed at Heidelberg University [5] in Germany. A photo of the chip is shown in Fig. 1. On its analog neural network core, it emulates up to 512 LIF neurons and $128\,\mathrm{k}$ synapses in analog circuits in parallel and in continuous time. Hardware synapses have 6-bit weights, which can be configured as inhibitory (negative sign) or excitatory (positive sign). The neurons communicate via digital spike events. Each neuron is parameterized individually to exhibit the desired dynamic. LI neurons can be realized by disabling the spiking mechanism. To facilitate training, BSS-2 provides a columnar ADC (CADC) allowing to read out neuron membrane voltages in parallel. Effectively, this allows ITL learning with surrogate gradients [7] where the forward pass is performed on-chip and weight updates are computed on the host computer [6].

For training our SNNs on the BSS-2 system we utilize the `PyTorch`-based [11] software framework `hxtorch.snn` supporting network execution on hardware and in simulation [12]. The BSS-2 software stack translates the high-level experiment description into a corresponding hardware configuration including stimulus data, uploads the experiment to an FPGA-based real-time experiment controller, and post-processes recorded output data.

Processing one sample y^t by the BSS-2 takes $30\,\mu\mathrm{s}$. In practical implementations, this can be speeded up, furthermore, many samples can be processed in parallel for achieving the required throughput.

Results

In Fig. 2B, we plot the BERs achieved with the 7-tap SNN equalizer/demapper, trained in software and on the analog BSS-2 system. For comparison, we also plot the BERs of software linear minimum mean square error (LMMSE) equalizers followed by a demapper with BER-optimized



C

net bit rate	200 Gb/s
FEC overhead	12 %
baudrate	112 GBd
wavelength	1270 nm
dispersion	−5 ps/nm/km
fiberlength	4 km

D

Net	Hidden layer width	Activation
SNN	40	LIF
ANN_1	40	ReLU
ANN_2	34, 10	ReLU

Fig. 2: (A) Simulated IM/DD link. Schematic taken from Arnold *et al.* [8]. **(B)** Comparison of BER results for transmission over a simulated IM/DD link with PAM4 constellations. **(C)** Considered IM/DD parameters. **(D)** NN parameters of demappers used. **(E)** Experiment observables of a single run recorded on BSS-2. **(F)** Weight matrices learned on BSS-2.

decision boundaries. As further references, we train software ANN equalizer/demappers with one and two hidden layers, see Fig. 2D. We observe that the simulated SNN performs better than the ANNs. The results show that the 7-tap SNN equalizer/demapper trained on BSS-2 outperforms the 7-tap LMMSE. For a BER of 2×10^{-3}, we observe a hardware penalty of less than 1 dB between the simulated SNNs and the BSS-2 SNN.

Figure 2E exemplifies the evolution of the hidden LIF neurons' analog membrane potentials v_j (upper) and their spikes (center) together with the readout traces v_k (lower) along the time ρ on the BSS-2 system. The hidden spikes push the membrane of the correct readout neuron $k = 2$ upwards while suppressing the traces of the other neurons $k = 0, 1, 3$, indicating a confident decision. The corresponding weight matrices W^{ih} and W^{ho} are depicted in Fig. 2F. The weights of the input neurons, receiving events from the central tap, are dominating since they encode the sample to classify, y^t.

Conclusions

In this work, we have implemented an SNN on the mixed-signal neuromorphic hardware system BrainScaleS-2 (BSS-2). While we observed a hardware penalty slightly below 1 dB at a BER of 2×10^{-3}, the BSS-2 SNN outperforms a simulated linear equalizer with the same number of taps, thanks to nonlinear processing.

The presented results confirm that neuromorphic hardware can provide the reliability required by signal processing in optical transceivers. Promising directions for future research include reducing the hardware penalty, reducing the architectural complexity and increasing the intrinsic speed of the SNN, and optimizing the input and output interfaces of the SNN. Furthermore, processing by the SNN must be parallelized. Also, the effective power consumption of neuromorphic signal processing should be analyzed and compared to digital processing.

In a future hardware implementation, spikes could be generated directly from the electrical signal coming from the photo diode, thereby replacing the power-hungry analog-to-digital converter (ADC). In this work, we have considered hard decision demapping. Another interesting direction is the design of an SNN equalizer/demapper with soft output.

Acknowledgements

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References

[1] B. J. Shastri *et al.*, "Photonics for artificial intelligence and neuromorphic computing", *Nature Photonics*, vol. 15, no. 2, 2021.

[2] S. Li, S. Dev, S. Kühl, K. Jamshidi, and S. Pachnicke, "Micro-ring resonator based photonic reservoir computing for PAM equalization", *IEEE Photonics Technology Letters*, vol. 33, no. 18, pp. 978–981, 2021.

[3] S. M. Ranzini, R. Dischler, F. Da Ros, H. Bülow, and D. Zibar, "Experimental investigation of optoelectronic receiver with reservoir computing in short reach optical fiber communications", *Journal of Lightwave Technology*, vol. 39, no. 8, pp. 2460–2467, 2021.

[4] W. Gerstner, W. M. Kistler, R. Naud, and L. Paninski, *Neuronal dynamics: From single neurons to networks and models of cognition*. Cambridge University Press, 2014.

[5] C. Pehle *et al.*, "The BrainScaleS-2 accelerated neuromorphic system with hybrid plasticity", *Frontiers in Neuroscience*, vol. 16, 2022, ISSN: 1662-453X. DOI: 10.3389/fnins.2022.795876. arXiv: 2201.11063 [cs.NE]. [Online]. Available: https://www.frontiersin.org/articles/10.3389/fnins.2022.795876.

[6] S. Schmitt *et al.*, "Neuromorphic hardware in the loop: Training a deep spiking network on the BrainScaleS wafer-scale system", 2017, pp. 2227–2234. DOI: 10.1109/IJCNN.2017.7966125. [Online]. Available: http://ieeexplore.ieee.org/document/7966125/.

[7] B. Cramer *et al.*, "Surrogate gradients for analog neuromorphic computing", *Proceedings of the National Academy of Sciences*, vol. 119, no. 4, 2022.

[8] E. Arnold *et al.*, "Spiking neural network equalization for IM/DD optical communication", in *Signal Processing in Photonic Communications (SPPCom)*, accepted, May 2022. arXiv: 2205.04263 [eess.SP].

[9] E. O. Neftci, H. Mostafa, and F. Zenke, "Surrogate gradient learning in spiking neural networks: Bringing the power of gradient-based optimization to spiking neural networks", *IEEE Signal Processing Magazine*, vol. 36, no. 6, pp. 51–63, 2019. DOI: 10.1109/MSP.2019.2931595.

[10] D. Kingma and J. Ba, "Adam: A method for stochastic optimization", *International Conference on Learning Representations*, Dec. 2014.

[11] A. Paszke *et al.*, "Pytorch: An imperative style, high-performance deep learning library", in *Advances in Neural Information Processing Systems 32*, H. Wallach, H. Larochelle, A. Beygelzimer, F. d'Alché-Buc, E. Fox, and R. Garnett, Eds., Curran Associates, Inc., 2019, pp. 8024–8035. [Online]. Available: http://papers.neurips.cc/paper/9015-pytorch-an-imperative-style-high-performance-deep-learning-library.pdf.

[12] E. Müller *et al.*, "A scalable approach to modeling on accelerated neuromorphic hardware", *Frontiers in Neuroscience*, 2022, Accepted. arXiv (preprint): 2203.11102 (cs.NE). [Online]. Available: https://www.frontiersin.org/articles/10.3389/fnins.2022.884128/full.