European Conference on Optical Communication (ECOC) 2022 ©
Optica Publishing Group 2022

CMOS Transceiver Circuits for Energy Efficient Silicon Photonic Interconnects

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Abstract *Energy efficient transceivers are necessary to scale optical interconnect performance well below 500fJ/b. We discuss our circuit design work in CMOS transmitter and receiver front-ends optimized for silicon photonic microring resonator-based wavelength division multiplexing interconnects.*

Introduction

Compact, power-efficient silicon-photonic transceivers that can be co-packaged utilizing the CMOS electronic ecosystem is a potential path toward addressing future data center bandwidth demands. The CMOS optical SERDES transceiver circuits that enable this must achieve energy efficiency levels well below 500fJ/b in order to support the subsequent growth in I/O bandwidth and comply with chip power constraints. Tight integration is also required between the photonic integrated circuit (PIC), which contains the high-speed modulators and photodetectors, and the electronic integrated circuit (EIC) that contains the optical SERDES transceivers to achieve this goal. This paper discusses our heterogeneous integration strategy and circuit design work in CMOS transmitter and receiver front-ends optimized for silicon photonic microring resonator-based wavelength division multiplexing (WDM) interconnects.

Heterogeneous WDM Transceiver Architecture

Fig. 1 shows the planned WDM optical transceiver architecture that is realized with heterogeneous integration between the silicon photonic and CMOS transceiver ICs. A WDM source provides multiple wavelengths that are edge coupled into a common silicon waveguide where a bank of ring modulators independently insert data onto the wavelengths before edge coupling the modulated signals out into a single-mode fiber. One of these wavelengths is dedicated as a forwarded-clock channel, which allows for reduced receive-side clocking complexity and the potential for improved high frequency jitter tolerance. On the receive side, the modulated wavelengths are also coupled into a common waveguide where a bank of ring drop filters select a wavelength per channel to direct onto a waveguide photodetector connected to the high-speed CMOS front-end.

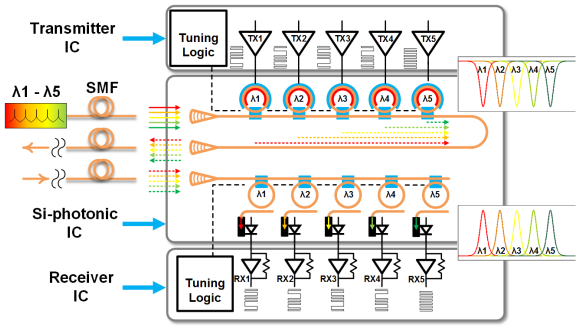
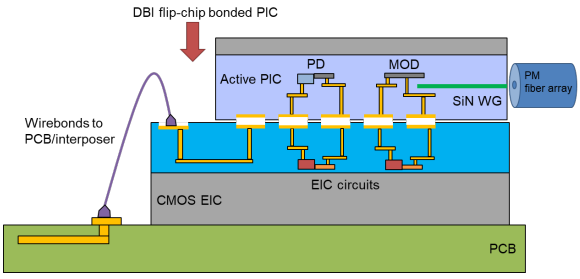
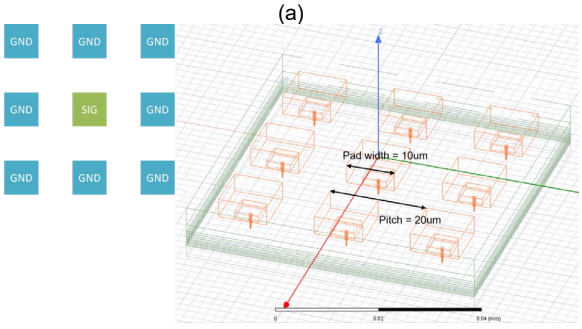


Fig. 1: Heterogeneous-integrated WDM optical transceiver based on silicon photonic microring modulators and drop filters.



(a)



(b)

Fig. 2: (a) DBI integration between PIC and EIC. (b) Modeling of DBI interconnect impedance.

As shown in Fig. 2(a), a high-density Direct Bond Interconnect (DBI) scheme [1] is planned for EIC and PIC integration in order to minimize interconnect parasitics that can have a dramatic impact on signal integrity and energy efficiency. 10μm square pads at a 20μm pitch are utilized in order to have a large number of I/Os in the transceiver circuit area. Modeling the CMOS and

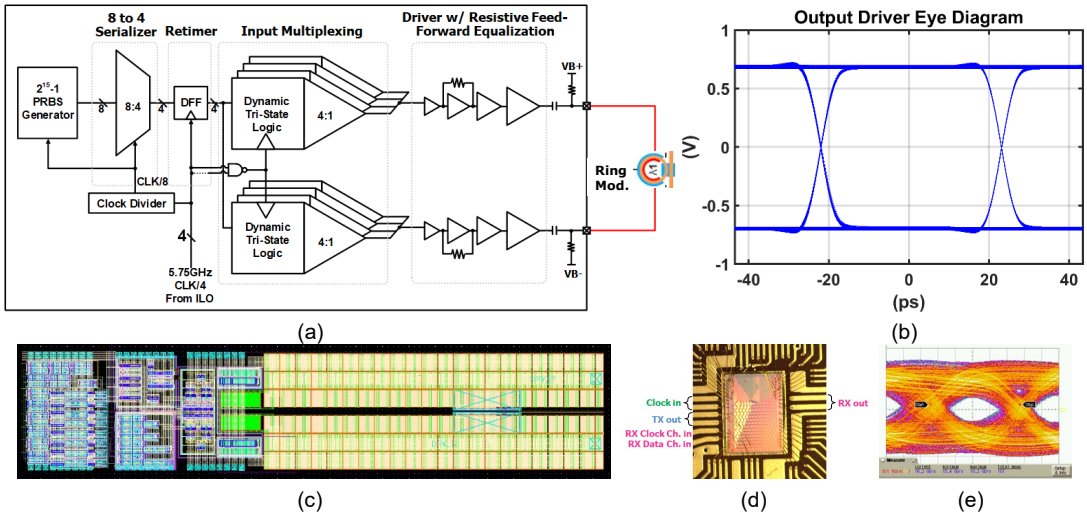


Fig. 3: Microring modulator transmitter: (a) block diagram, (b) simulated 23Gb/s eye diagram, (c) circuit layout, (d) 28nm CMOS die micrograph, and (e) measured electrical 16Gb/s eye diagram.

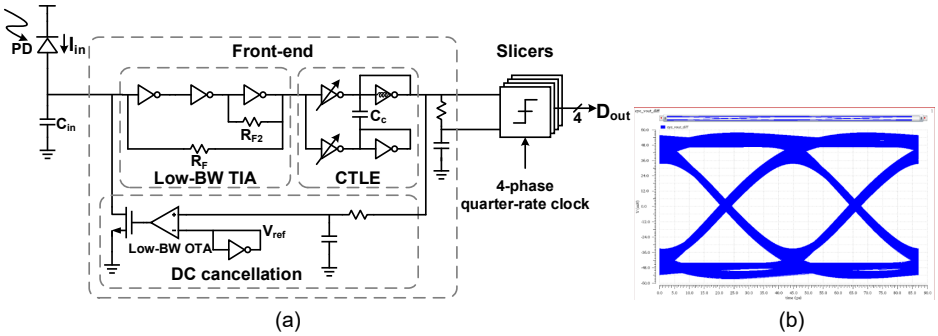


Fig. 4: Inverter-based optical receiver: (a) block diagram and (b) simulated 23Gb/s eye diagram at slicers' inputs.

PIC metal stackup through the DBI interface with Ansys Q3D yields 5.5fF total capacitance from the interconnect (Fig. 2(b)). The EIC is placed on bottom in order to leverage the CMOS chip metallization, which has more layers for signal routing and thicker layers for better power supply integrity. 3D LVS is utilized to verify the interface between the PIC/EIC [2]. Wirebonds on the EIC perimeter are utilized to connect the 3D integrated PIC/EIC to the PCB/interposer.

Low-Voltage Microring Modulator Transmitter

The CMOS optical transmitter shown in Fig. 3 operates with simple PAM-2 modulation and performs an 8:1 SerDes operation to interface with parallel data clocked at a reasonable 2.875GHz at the maximum 23Gb/s data rate. Significant savings in clocking power is achieved with a quarter-rate architecture that allows operation of the majority of the transmitter circuitry on a low 0.7V dynamic voltage frequency scaling (DVFS) supply. This low-voltage operation is enabled by utilizing an efficiency dynamic tri-state logic serializer with low output capacitance and simple resistive feed-forward equalization in the predriver stages after the mux. The CMOS inverter-based output driver provides a nominal swing of twice the DVFS supply ($1.4V_{ppd}$) and is AC-coupled to the microring modulator to allow for bias point optimization. This swing would yield an ~10dB extinction ratio when driving a microring modulator with sub-20fF capacitance [3]. The complete transmitter has a simulated power consumption of 2.8mW at 23Gb/s operation under this condition, which results in 122fJ/b energy efficiency. An optical transceiver test chip is fabricated in 28nm CMOS and includes several transmitter channels designed for both high-density bonding and wirebond testing. Each transmitter channel occupies 20μm X 100μm area. Initial electrical characterization shows a relatively open 16Gb/s eye, with operation at higher speed limited by the high-frequency electrical PCB trace loss.

Inverter-Based Optical Receiver

Fig. 4(a) shows the all-inverter-based optical RX architecture. A low-bandwidth TIA converts the single-ended PD input current to an output voltage that is equalized by the CTLE. An RC low pass filter then generates a pseudo-differential signal for the four slicers driven by 4-phase

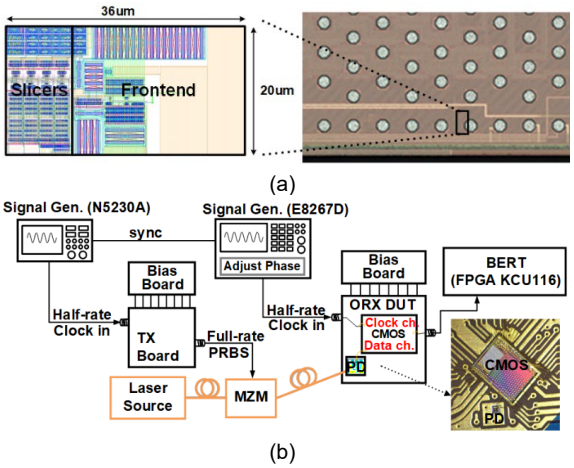


Fig. 5: (a) Optical receiver layout and chip micrograph and (b) optical test setup.

quarter-rate clocks. Stabilization of the output common-mode voltage is achieved with a DC cancellation loop.

While nanometer CMOS devices can have a high gain-bandwidth product, generally the gain from a single inverter stage is relatively low. The high-speed low-gain amplifier can make it difficult to realize the desired second order closed-loop response with a single-stage TIA and further limit the achievable R_F value, resulting in higher input-referred noise. The proposed design addresses this by placing the post-amplifier in the TIA feedback loop to allow for an increased TIA feedback resistance. Through proper choice of the R_{F2} value, the poles associated with the extra stages are placed at a high enough frequency to not impact the overall frequency response. This allows for approximately the same overall transimpedance, bandwidth, and power consumption as a conventional design. The input-referred noise from the TIA feedback amplifier is also roughly equal, as it is dominated by the size/power of the input stage. Conversely, the input-referred noise power from the feedback resistor is significantly reduced by a factor of $g_m R_{F2}$ in the multi-stage amplifier design. Further noise reduction is achieved by utilizing a subsequent inverter-based CTLE. This topology decouples the TIA noise and bandwidth requirements, allowing for the TIA feedback resistance to be further increased for higher gain and lower noise.

The optical receiver is designed in the same 28nm CMOS process as the transmitter. The design was optimized to operate at 23Gb/s and interface with a 20fF waveguide photodetector through the low-capacitance DBI interface. A simulated -20dBm OMA sensitivity under this condition, with a 100mV_{ppd} swing delivered to the slicers (Fig. 4(b)). The power consumption is

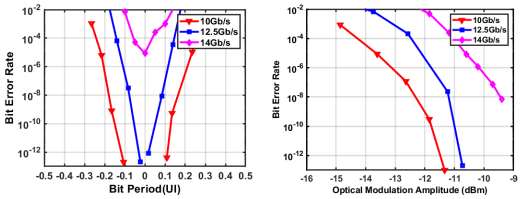


Fig. 6: (a) Measured receiver BER timing margin curves with OMA = -10.7 dBm and (b) sensitivity curves.

1.7mW, which results in 74pJ/b energy efficiency. Fig. 5 shows the chip micrograph and layout details of the optical receiver, which occupies 720μm^2 area. Initial optical testing is performed with a 0.6 A/W InGaAs PD wire bonded to the optical receiver input. This results in a large 150 fF total combined input capacitance from the PD and bonding pads and reduced data operation. Fig. 6 shows measured timing bathtub and sensitivity curves at 10 Gb/s, 12.5 Gb/s, and 14 Gb/s. The 12.5 Gb/s OMA sensitivity at BER=10^{-12} is -10.7 dBm with a 0.04 UI timing margin.

Conclusion

This paper presented our ongoing circuit design work in CMOS transmitter and receiver front-ends optimized for silicon photonic microring resonator-based wavelength division multiplexing interconnects. The tight integration offered by the DBI interface, coupled with the DVFS transmitter and a multi-stage TIA and CTLE-based receiver, allow for potential sub-200fJ/b energy efficiency. While ring tuning power was not addressed, our future plans involve utilizing athermal microring structures to address this [4].

Acknowledgements

This work was support in part by the DARPA PIPES program, ARO under Grant W911NF1910470, and by DoE UAI Consortium under Grant DE-SC0019582, Grant DE-SC0019526, and Grant DE-SC0019692.

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