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Low Power Four-Dimensional Multi-Level Coding

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Abstract *A novel four-dimensional multi-level coding architecture is proposed in which only 1.5 bit/complex symbol are soft decoded, leading to an additional 25% power-savings compared to existing coding architectures. Simulation results confirm that these savings are achieved without performance loss, while maintaining compatibility with probabilistic-constellation-shaping. ©2022 The Author(s)*

Introduction

The forward error correction (FEC) modules in fiber-optic communication transceivers are very power-hungry, consuming upwards of 30% of the total operating power budget. As data rates rise and transceivers are packaged more densely, management of power consumption and heat dissipation becomes increasingly challenging. This has motivated the design of architectures and algorithms for low-complexity, low-power FEC modules [1-7].

Two types of FEC codes are often seen in fiber-optic communication systems: hard-FEC and soft-FEC. Hard-FEC decoders in general consume much less power than soft-FEC decoders, as only binary values are processed as opposeed to non-binary log-likelihood-ratios (LLRs). However, on additive-white-Gaussian noise (AWGN) channels, with the same input bit-error ratio (BER) threshold, hard-FEC often pays the price of higher overhead (OH) than the soft-FEC counterpart. The gap between a carefully designed hard-FEC and soft-FEC is large when the OH is around 1, and diminishes as the OH approaches 0 and infinity. As industry pushes for higher spectral efficiency (SE), higher-order quadrature amplitude modulation (QAM) formats (e.g., 16-QAM, 64-QAM, etc.) are used, which often result in higher pre-FEC BER and higher FEC OH. More and more systems have employed soft-FEC for better performance.

Conventional bit-interleaved coded-modulation (BICM) provides the same level of protection to all bits in the constellation label. To reduce power consumption in BICM, one may choose a concatenated FEC structure [1,2], in which an inner soft-FEC is used to bring the BER down to the order of 10^{-3} or 10^{-4} (error reduction only), and a high-rate outer hard-FEC corrects the residual errors to a BER below 10^{-15}. The power saving comes from fewer required iterations due to relaxed output BER requirement of the soft-FEC in the concatenated scheme, compared to a soft-FEC only scheme. The emerging low-complexity high-coding-gain hard-FEC designs such as staircase codes [8] and zipper codes [9] also make such architectures more attractive. One may further reduce the decoding power by utilizing multi-level-coding (MLC), which can reduce the number of bits processed by the soft-FEC decoder and hence lower the power consumption [3-7]. In MLC systems, different bit levels exhibit different BER, and only the ones with higher BER need to be decoded by a soft-FEC. In this case, the soft FEC may be used to perform error correction [5], or error reduction only [3,4,6,7] and the residual errors will be corrected by the hard-FEC. The works in [3-6] uses the soft-FEC to decode 2 bits/complex symbol, while the proportion of soft-FEC decoded bits may vary in [7]. When 16-QAM is used, the expected power saving compared to BICM is roughly 50% in [3-6], and 42% in [7].

Another popular technology in fiber-optic communication systems is probabilistic-constellation-shaping (PCS) [10,11]. PCS provides two benefits: given a modulation format, it can be used to optimize the input distribution to achieve higher mutual information between the transmitted and received symbols; for different transmission distances and signal-to-noise-ratio (SNR) levels, it can be used to achieve rate adaptation without changing the modulation format or FEC rate. Therefore it is important for the proposed low-power FEC design to be compatible with PCS, and we investigate its performance over a large range of PCS levels.

We propose a new 4-dimensional (4D) MLC structure that only requires 1.5 bit/complex symbol to be soft-decoded. This is equivalent to ~62.5% power saving in soft-FEC decoder, compared to BICM, and addition 25% power saving compared to the MLC structure in [3-6]. We also demonstrate the performance of the 4D-MLC over a large range of SNRs when combined with different PCS levels, and show that the gap to Shannon limit is less than 1.7 dB.

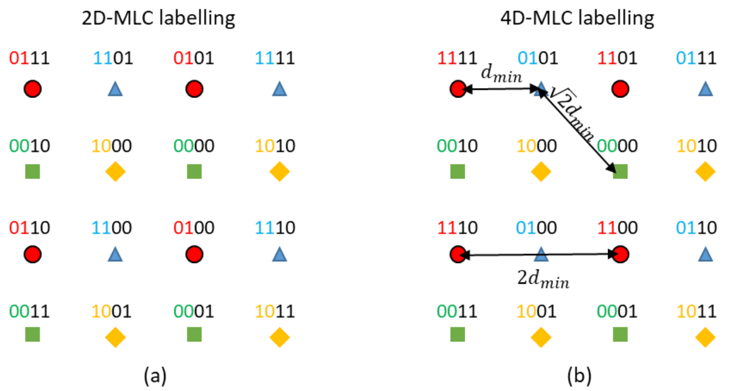

Fig. 1: 16-QAM constellation labelling schemes for (a) 2D-MLC and (b) 4D-MLC.

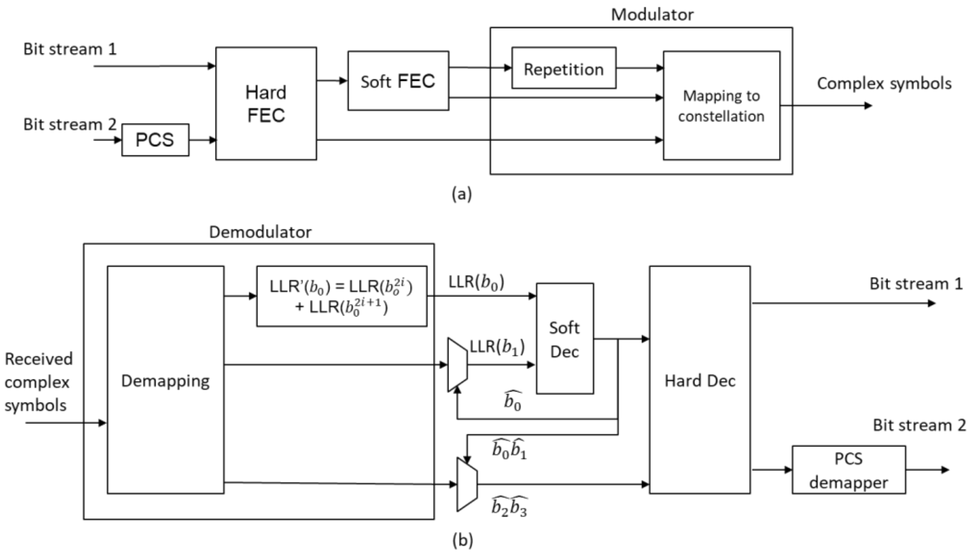

Fig. 2: Block diagram of the proposed 4D-MLC system: (a) transmitter; (b) receiver.

4D-MLC vs. 2D-MLC

In the remainder of the paper, the MLC schemes proposed in [3-6] are referred to as the 2D-MLC systems. Potential performance advantages of the 4D-MLC scheme was discussed in [12], but with a non-binary LDPC inner code with very high decoding complexity. We propose a new 4D-MLC system that encodes/decodes two complex symbols at a time, using the conventional QAM constellations and binary FECs. These two complex symbols can be two symbols in different time slots or two symbols across x and y polarizations. Without loss of generality, we use symbols at time $2i$ and $2i+1$, denoted as S^{2i} and S^{2i+1}. We focus on 16-QAM in this paper; however, the proposed concept can be easily expanded to higher order modulation formats such as 64-QAM.

The constellation labelling scheme used in 2D-MLC is equivalent to what is illustrated in Fig. 1 (a) [3-6]. Let b_0, b_1, b_2, and b_3 denote the most-significant-bit (MSB), the second MSB, the second least-significant-bit (LSB), and the LSB, respectively. The two MSBs (b_0, b_1) set-partition the constellation to four subsets (shown with different shapes in Fig. 1 (a)). Let d_{min} be the minimum Euclidean distance in the original constellation. Conditioned on knowing (b_0, b_1), the minimum Euclidean distance in each of the subsets is $2d_{min}$, which leads to a much lower BER in (b_2, b_3) than in (b_0, b_1). Only (b_0, b_1) are protected by the soft-FEC, while (b_2, b_3) are protected by the hard-FEC. This leads to 50% throughput reduction in the soft-FEC compared to BICM systems.

The proposed 4D-MLC follows the labelling scheme illustrated in Fig. 1 (b). There are 16 constellation points in the top level. In the second level, the points are set-partitioned to two subsets by b_0, where the first subset consists of the circle and diamond points, and the second subset consists of the square and triangle points. In the third level, each subset is further set-partitioned to two smaller subsets by b_1, resulting in four subsets in total (shown with different shapes in

Tab. 1: Simulation setup for 2D and 4D-MLC. The inner soft-FEC used are LDPC codes with maximum of 8 layered-decoding iterations. The outer hard-FEC used are zipper codes with triple-error-correcting BCH component codes (t = 3).

	Soft FEC	Soft-FEC OH	Hard-FEC	Hard-FEC OH	Overall coding OH
2D-MLC	LDPC (49152, 29184)	68%	Zipper (t = 3)	4.92%	31.54%
4D-MLC	LDPC (50688, 31488)	61%	Zipper (t = 3)	5.03%	43.3%

Fig. 1 (b)). The minimum Euclidean distance in each subset within the second level is $\sqrt{2}d_{min}$ conditioned on knowing b_0, and it is $2d_{min}$ in the each subset within the third level conditioned on knowing (b_0, b_1). With such a labelling design, the bits can be separated to three groups in descending order of BER: b_0, b_1, and (b_2, b_3).

Due to implementation constraints, only two FEC encoder/decoder pairs are allowed in the FEC module. To offer better error protection to b_0, we propose to map two complex symbols at a time, S^{2i} and S^{2i+1}, with labels $\left(b_0^{2i}, b_1^{2i}, b_2^{2i}, b_3^{2i}\right)$ and $\left(b_0^{2i+1}, b_1^{2i+1}, b_2^{2i+1}, b_3^{2i+1}\right)$, respectively. The modulator takes in seven FEC-encoded bits at a time to produce S^{2i} and S^{2i+1}, by generating $b_0^{2i+1} = b_0^{2i}$ for all i, i.e., by repetition coding b_0^{2i}. Among the seven FEC-encoded bits, $(b_2^{2i}, b_3^{2i}, b_2^{2i+1}, b_3^{2i+1})$ are hard-FEC encoded only. Although b_0^{2i} and (b_1^{2i}, b_1^{2i+1}) are both hard-FEC and soft-FEC encoded, they are not encoded by the same soft-FEC codeword, because they need to be decoded sequentially in the decoder. The transmitter encoding block diagram of the proposed 4D-MLC is shown in Fig. 2 (a). On the decoder side, the log-likelihood-ratio (LLR) of b_0^{2i} and b_0^{2i+1} are computed based on the received symbols, denoted as $LLR(b_0^{2i})$ and $LLR(b_0^{2i+1})$. Since by design $b_0^{2i} = b_0^{2i+1}$, an updated LLR can be assigned to them by computing $LLR'\left(b_0^{2i}\right) = LLR\left(b_0^{2i}\right) + LLR(b_0^{2i+1})$. This summation is considered to have negligible complexity compared to the soft decoder. The quantity $LLR'(b_0^{2i})$ is passed to the soft FEC decoder along with $LLR\left(b_1^j\right)$'s, for some $j < 2i$ with b_0^j's already decoded by the soft decoder. Let $\widehat{b_0^{2i}} = \widehat{b_0^{2i+1}}$ be the decision of the soft decoder for the MSBs of the S^{2i} and S^{2i+1}. Conditioned on $\widehat{b_0^{2i}}$ and $\widehat{b_0^{2i+1}}$ one may compute $LLR\left(b_1^{2i}\right)$ and $LLR\left(b_1^{2i+1}\right)$, which are passed to the soft decoder along with $LLR'(b_0^{2k})$'s, for some $k > i$.

Let $\widehat{b_0}$ and $\widehat{b_1}$ be the soft decoder decisions on the two MSBs of any symbol. Conditioned on $(\widehat{b_0}, \widehat{b_1})$, one may compute $\widehat{b_2}$, and $\widehat{b_3}$ based on the received symbol, and errors in $(\widehat{b_0}, \widehat{b_1}, \widehat{b_2}, \widehat{b_3})$ can be corrected by the hard decoder (Fig. 2 (b)).

Simulation Results

The performance of the proposed 4D-MLC architecture is tested by simulation over AWGN channels. The base constellation used is 16-QAM, and ideal Maxwell-Boltzmann shaping [13] is used in the PCS block. The soft FECs are low-density-parity-check (LDPC) codes with maximum of 8 layered-decoding iterations, and the hard FECs are zipper codes with input BER threshold of $\sim 1.5 \times 10^{-3}$ (the OHs are shown in Table 1). Since 4D-MLC pays extra OH for the repetition code, it has a higher overall coding OH. The PCS level is adjusted accordingly to achieve the same SE for both 2D- and 4D-MLC systems. The required SNR levels for a range of SEs are found by simulation, which are also compared with the capacity of complex AWGN channel (Shannon limit)

$$C = \log_2\left(1 + \frac{P}{N}\right),$$

in Fig. 3, where P is the signal power, and N is noise power [14]. Over the tested range of SE, 4D-MLC shows no performance loss compared to 2D-MLC and it is within 1.7 dB gap to Shannon limit. 4D-MLC only requires 1.5 bit/complex symbol to be decoded by the soft-FEC. It offers 62.5% soft-FEC power saving compared to BICM, and additional 25% power saving compared to 2D-MLC.

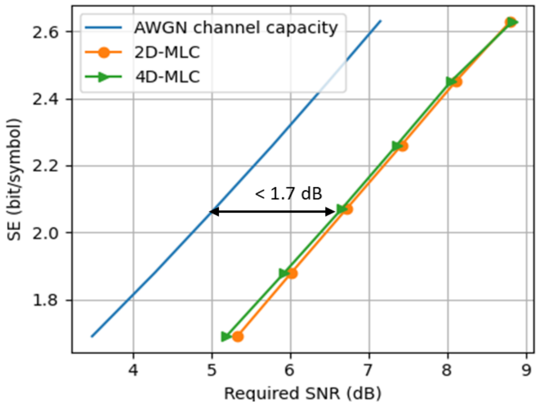

Fig. 3: Required SNR comparison of 2D-MLC vs. 4D-MLC.

Conclusion

We proposed a novel 4D-MLC architecture for fiber-optic communication systems. It is compatible with PCS, and only requires 1.5 bit/complex symbol to be soft-decoded. It is able to offer ~25% power saving compared to existing 2D-MLC architectures without performance loss.

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