110GHz Through-Silicon Via's Integrated in Silicon Photonics Interposers for Next-Generation Optical Modules

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Abstract *We report Through-Si Via's (TSV) with RF bandwidth beyond 110GHz integrated in a Silicon Photonics interposer, targeting next-generation optical modules operating at 100Gbaud data rates. Showcasing low RF loss, high-quality data transmission is demonstrated at 112Gb/s NRZ data rate for test structures including two TSVs.*

Introduction

Future intra-datacenter links are demanding 212 Gb/s 4-level pulse amplitude modulation (PAM-4) lane rates [1]. Besides ~70GHz optical components, electrical I/O with low radio frequency (RF) loss over 70 GHz is also required. A hybrid CMOS/Si Photonics assembly approach using silicon photonics interposers with integrated through-silicon-via's (TSV) [2], capable of a high-quality transmission for 100Gbaud data, can enable next-generation pluggable modules and co-packaged optics, as shown in Fig.1. To the best our knowledge, high-frequency performance and high-data rate signal characterization results at 100Gbaud have not yet been reported for TSVs in Si photonics interposers.

In this paper, RF characterization up to 110 GHz of the TSV and a calibrated compact model are presented, assisted by full-wave electromagnetic (EM) simulations. Following the RF analysis of the TSVs, eye-diagrams at 112 Gb/s non-return-to-zero (NRZ) signal of the same TSV test structures are also measured and analysed.

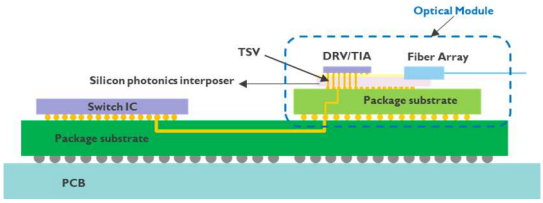
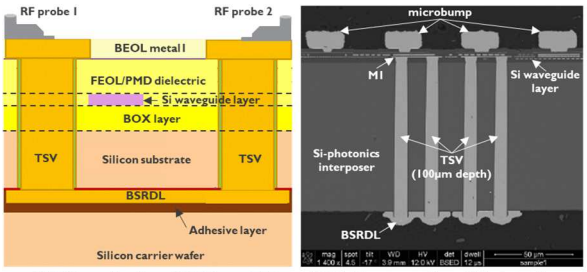


Fig. 1: Schematic view of co-packaged optics

TSV RF Characterization

3D stacked interconnects based on two TSVs and a back-side redistribution-layer (BSRDL) transmission line are fabricated in silicon photonics interposers using 300mm silicon-on-insulator (SOI) wafers with a 220nm-thick Si waveguide layer and 2µm-thick buried-oxide [3]. Fig.2 shows a cross-sectional view of the interconnect and photo of fabricated TSV with 11µm diameter and 100µm depth. To make an electrical contact for RF and high-speed measurements, a 0.5µm-thick Cu metal 1 (M1) layer are deposited in back-end-of-line (BEOL) process to form RF pads and access lines to the TSVs. The front-side interface is achieved with stacking the SOI interposer attached on a carrier wafer through an adhesive layer [3][4].



(a) Schematic view of TSV-based 3D stacked interconnect test structure (not in scale)

(b) SEM cross-section of Si-photonics interposers (micro bumps are shown as a full process flow of imec Si-photonics platform)

Fig. 2: A layer structure of 3D stacked interconnects and SEM cross-section of the fabricated silicon-photonics interposer, showing TSVs connected to BSRDL.

Fig. 3 depicts a microphotograph of the main structure of the TSV interconnect. A 100µm-long M1 coplanar waveguide (CPW) transmission line is designed to be 50 Ω characteristic impedance. The signal line is implemented with a single TSV and is connected with BSRDL CPW line. The materials and process parameters of the interconnect are listed in table 1.

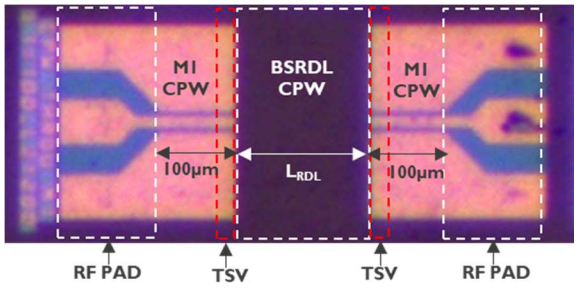


Fig. 3: A microphotograph of test structure of the 3D stacked interconnect.

The interconnect RF model is built in a commercially available full-wave EM simulator (HFSS) as illustrated in Fig. 4. The 3D stacked

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Tab. 1: 3D interconnect parameters and materials

Silicon resistivity	10 Ωcm
TSV diameter	11 µm
TSV liner thickness	0.7 µm
TSV depth	100 µm
Adhesive layer thickness	30 µm
Metal 1	Cu, 0.5 µm thickness
BSRDL	Cu, 3 µm thickness

interconnects of M1 CPW-TSVs-BSRDL CPW are measured up to 110 GHz as shown in Fig. 5, excluding influences of the RF pads by de-embedding. The return loss of the 3D interconnect with 200µm-length BSRDL is better than 11dB and an insertion loss of 1.8dB is achieved at 110 GHz. The HFSS 3D model of the interconnet shows a excellent match with the measured data of 3 different lengthes of BSRDL 100µm, 200µm and 1000µm across the entire frequency range up to 110GHz.

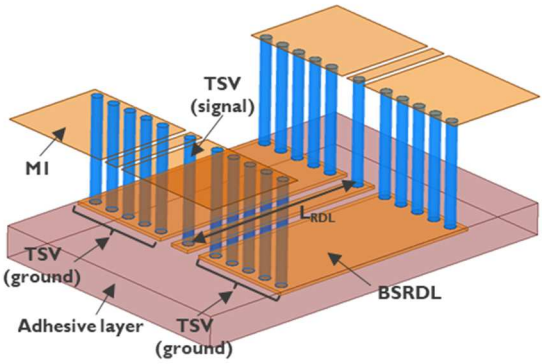

Fig. 4: EM **s**imulation model setup of the 3D stacked interconnects.

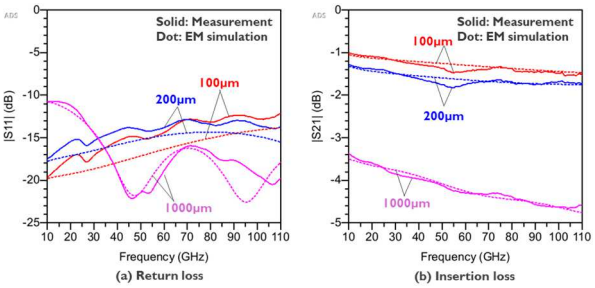

Fig. 5: Measured and simulated 3D stacked interconnects (L_{RDL}=100µm, 200µm and 1000µm)

To ensure RF losses of M1 CPW transmission line, M1 CPW test structures of 450µm, 950µm and 2950µm lengths without TSVs and BSRDL CPW line are also measured as shown in Fig. 6. The M1 CPW lines achieve the return loss of below 25dB up to 110GHz. The 950µm-long M1 CPW shows an insertion loss of 1.4dB at 110GHz.

TSV compact modeling

For circuit simulation use, a T-type lumped

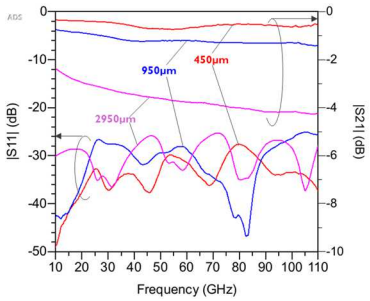

Fig. 6: Measured return and insertion losses of metal1 CPW line (450µm, 950µm and 2950µm length)

element equivalent model of a single TSV can represent the TSV RF characteristics, as illustrated in Fig. 7. In addition to basic R/L/G/C elements for a general distributed transmission line model [5], a series connection of a resistor and an inductor is connected in parallel with the resistor to model a frequency-dependent resistance. An extra capacitor introduced by TSV liner material is also connected to substrate networks.

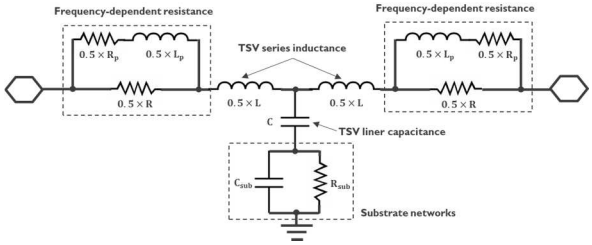

Fig. 7: TSV lumped element equivalent circuit model

The HFSS simulation deck of the 3D stacked interconnect (validated by the measured data) is used to extract R/L/G/C values of a single TSV [6], since there is no test structure of the single TSV to be measured with RF pad. In Fig. 8, the extracted R/L/G/C values with a process-related variation of TSV oxide liner thickness from 0.5um to 0.9um are compared to the TSV model with parameters specified in table 2. The RF performances of the single TSV model are also validated up to 110 GHz by excellent agreement with the HFSS simulated return and insertion losses shown in Fig. 9.

Tab. 2: TSV model parameters (Liner thickness=0.7µm)

Parameter	Value	Description
R	0.95 Ω	High-frequency resistance
L	46.5 pH	TSV series inductance
C	110 fF	TSV oxide liner capacitance
Rsub	370 Ω	Substrate resistance
Csub	28 fF	Substrate capacitance
Rp	34 mΩ	Low-frequency resistance
Lp	3.8 pH	Frequency-dependent component of resistance

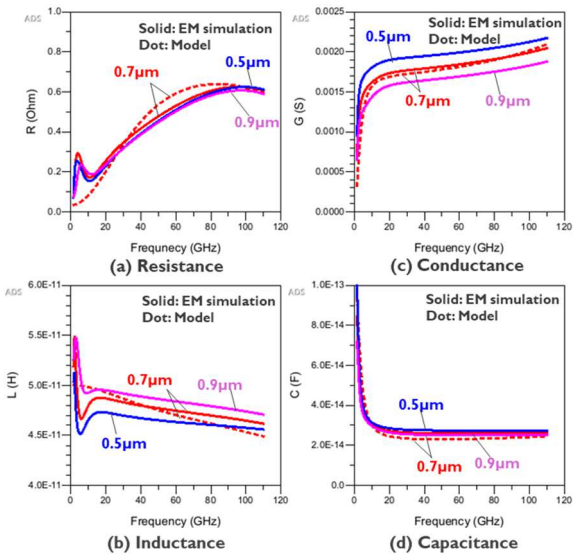

Fig. 8: RLGC extraction and modeling of the TSV (liner thickness=0.5μm, 0.7μm and 0.9μm)

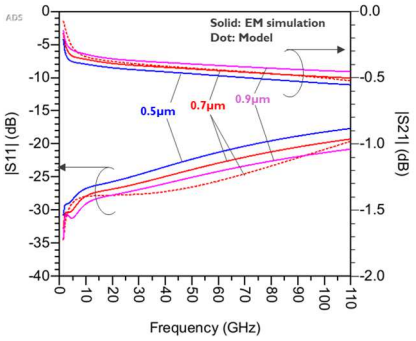

Fig. 9: TSV RF performances of EM simulations and RLGC model

TSV high-speed signal characterization

To further validate the high-speed signal capabilities of the TSV interconnects, eye-diagrams are evaluated with launching a 112 Gb/s NRZ input signal. Our high-speed bit-pattern generator and RF cabling provides an NRZ signal with 503fsec jitter RMS and signal-noise-ratio (SNR) of 4.78 and peak-to-peak amplitude of 400mV at 112 Gb/s. Fig. 10 shows the measured eye-diagrams of launched and received signals through the 3D interconnects with 200μm-BSRDL. The received signal maintains an eye opening at 112Gb/s NRZ through the 3D interconnects, even though the measured RF insertion loss of the 3D interconnect (TSVs and BSRDL including RF pads) is reflected in a degradation of eye amplitude (a mean value of a peak-to-peak amplitude at eye window).

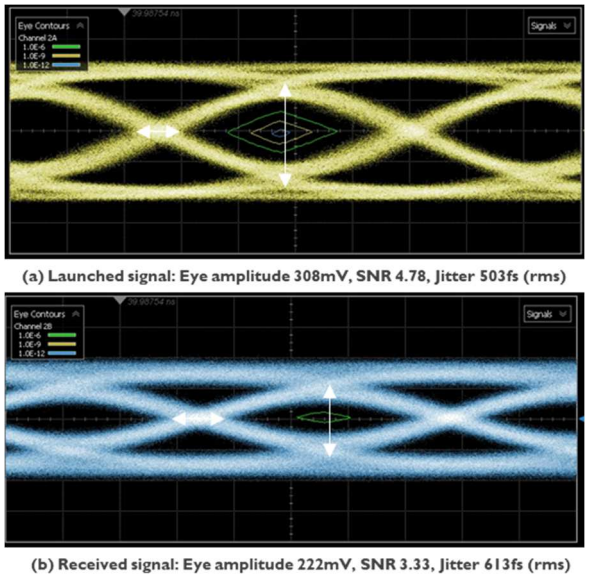

Fig. 10: Measured NRZ eye-diagrams at 112 Gb/s of the launched (top) and received signal (bottom) through the 3D stacked interconnect in Fig. 3 (L_{RDL}=200μm)

The 3D interconnects with different BSRDL lengths up to 1.5mm are also tested. Fig.11 shows jitter RMS, SNR, and eye amplitude of launched and received signal as a function of BSRDL length. The jitter RMS significantly increases as the BSRDL length is large, while SNR and eye amplitude degrade proportionally with the length.

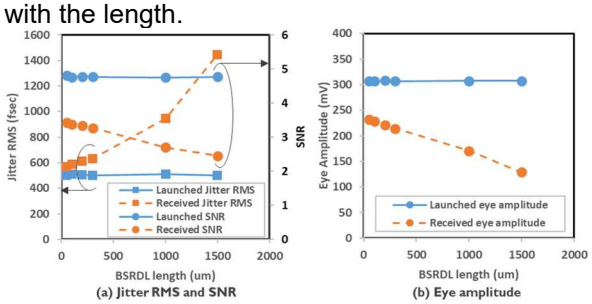

Fig. 11: Measured Jitter RMS, SNR, and eye amplitude of eye-diagrams through the 3D stacked interconnect (L_{RDL}=50 μm~1500μm)

Conclusions

We have demonstrated high-speed RF TSVs integrated in silicon photonics interposers with 0.5dB insertion loss at 110GHz. The TSV lumped element model has been developed by RLGC fitting to the experimentally validated EM simulation results up to 110GHz. The large-signal data transmission at 112Gb/s NRZ has revealed a clear open eye-diagrams, further illustrating the RF capability for beyond 100Gbaud data link applications.

Acknowledgements

This work has been supported by imec's industry-affiliation R&D program on Optical I/O.

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