Novel Semiconductor Optical Amplifier with Large Gain and High Saturation Output Power

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Abstract A novel semiconductor optical amplifier (SOA) design achieving large gain and high saturation output power without reaching excessive power consumption level is presented. Small-signal gain above 35 dB and 22 dBm high saturation output power were measured at 1.3 A biased current.

Introduction

With the current demand for increased capacity in optical communication systems, versatile, high performance and low cost optical amplifiers are required, either to extend the optical bandwidth of amplified links (in metropolitan or long-haul systems), or to allow for optical amplification in unamplified links (in optical access or inside data centres). Semiconductor Optical Amplifiers (SOA) are extremely versatile, but suffer from non-linearity in the saturated regime. To overcome this, large saturation power SOA have been developed. The highest reported output power from an InP discrete SOA was achieved using a slab coupled optical waveguide (SCOW) design with a low optical confinement quantum wells scheme [1] however at the expense of the gain. Indeed, this design provides nearly watt-level 3-dB saturation output power (P_{sat}) with only 13.5 dB gain. In addition, this performance was achieved with 5 A injection current, implying a high power consumption of the device, and consequently of the thermoelectric cooler (TEC). Another advanced design was reported for an InP/InGaAsP SOA with 3 thin quantum wells (MQW) [2]. The reported chip saturation output power at 1A is 23 dBm but with 15 dB gain. As described in [3], there is always a trade-off between gain, saturation power and power efficiency in low-confinement SOAs to be made.

In order to mitigate the trade-off in a single SOA structure, we present in this paper a new design of MQW SOA made of two sections. The SOA first section with an upper cladding taper was designed to meet the high gain requirement while the SOA second section was designed to meet the high saturation output power requirement. We first analyse the main factors ruling the gain and the saturation output power, then we present the chip design followed by the characterization results. We demonstrate up to 40 dB small-signal chip gain and 22 dBm chip saturation output power at 1.3 A. Using the product G_0 x P_{sat} as a figure of merit [3], our new design is compared with the results of [1] and [2].

Analysis of SOA gain and P_{sat}

The small-signal gain G_0 of the SOA can be expressed as follows

$$G_0 \propto \exp((\Gamma * g_{mat} - \alpha) * L) \quad (1)$$

with Γ the optical confinement in the active region, g_{mat} the gain material, α the propagation losses per cm, and L the chip length.

By ignoring the propagation losses, the Spatial Hole Burning and the Amplified Spontaneous Emission, P_{sat} is found proportional to the following product:

$$P_{sat} \propto h\nu \frac{A}{\Gamma} \frac{1}{a_1 \tau} \quad (2)$$

with A the cross-section area (width × thickness) of the active region, Γ the optical confinement in the active region, a_1 the material differential gain, and τ the carriers lifetime.

As it can be seen from expressions (1) and (2), the confinement factor is one of the main parameters. Large P_{sat} requires low confinement factor. If high gain is also targeted, then long SOA and large currents should be used. Therefore, having a section with high confinement and a section with low confinement, a high gain and high P_{sat} could be achieved with moderate currents and chip length.

SOA dual-section design

The section with high output saturation power is achieved with low optical confinement targeted by inserting a thick under-cladding layer below the active layer [1] [4] [5], in the n-doped part of the SOA stack. The refractive index of this cladding layer has to be slightly larger than the one of InP, in order to attract the optical mode in the n-doped layers, away from the lossy p-doped layers. This section is referred here after as STD or S. Note that the SOA with one section is made of this high saturation output power section and is referred here after by standard SOA.

The section with high gain is achieved with high optical confinement by inserting an upper cladding (UC) layer over the active layer, in the p-

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doped part of the SOA stack. The refractive index of the UC layer is higher than the p-doped InP layer so that it can attract the optical mode to compensate the traction from the slab leading to a large confinement factor in the quantum wells.

However, in order to achieve a design where gain and saturation output power of both sections are balanced, the upper cladding section shouldn't be saturated. Note that, in the latter case, the output power approaches saturation output power only near the output of the SOA, so P_{sat} can be calculated with Eq. (2), where A and Γ are given by the output section.

SOA Fabrication

Standard SOA using a thick under-cladding layer were made using InGaAsP multi-quantum wells for the active region. The active stripe was tilted by 7deg with respect to the cleaving direction to reduce optical feedback, and the facets were Anti-Reflection coated.

Semi-insulating buried heterostructure (SIBH) process was used for the SOA fabrication in order to achieve good heat dissipation and circular modes by burying the waveguide in an insulating and heat-conductive material. During a first epitaxial growth, the under-cladding (n-doped) InGaAsP slab, the active region and the p-doped upper-cladding layer were grown on an InP substrate. Then the waveguide was etched into the slab followed by an epitaxial regrowth of an insulating layer of InP on the sides of the waveguide.

For the high P_{sat} section, the upper-cladding layer was selectively etched. Between both sections, the upper cladding layer was partially etched to form a taper along the interface between the two sections of the device, as illustrated in Fig.1. Section U refers to the section with the UC layer, and section S to the section with the standard structure i.e. without the UC layer. At section U input, the ridge width is smaller than section S output ridge width. Note that the enlargement of the output ridge width also helps to increase the saturation output power.

The fundamental optical mode TE0 of both sections is displayed in Fig. 2, showing the difference of the optical mode confinement in the quantum wells.

SOA measurements

The SOA devices were tested mounted on carriers and were made with different UC section lengths (0, 1.7, 2.3mm) over a 4 mm total chip length corresponding to 0, 43% and 56% ratio of the total length and referred to here after as STD, 43% UC and 56% UC respectively. The STD device was used as reference to understand the impact of the UC section. The devices were

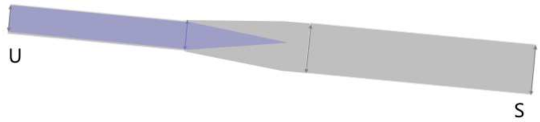

Fig. 1: SOA top view

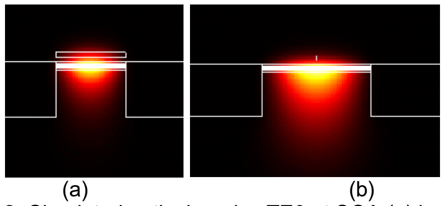

Fig. 2: Simulated optical modes TE0 at SOA (a) input U and (b) output S

tested under controlled temperature at 20°C. The biased current was set at 1.3 A. Optical fibre lens assembly was used for the light coupling into the waveguide inducing 1 dB coupling loss per facet. For the small-signal measurements, the input power was set at -25 dBm. The measured and simulated small-signal gain spectra are shown in Fig. 3. In the legend, "UC→STD" means that optical signal is injected from the upper-cladding side, "STD→UC" means that the optical signal is injected from the standard side.

With the 56% upper-cladding structure, the highest chip gain is achieved and it reaches ~40 dB at 1575 nm, and is 10 dB higher than the standard design. The 3-dB gain bandwidth is measured around 90 nm with all the designs, covering a good section of C and L bands. The measured chip noise figure NF is 4.5 dB at 1600 nm with the standard device, and 0.3 dB worse with the upper-cladding devices due to the higher loss of the UC section. Based on the measurement of the small-signal gain at different biased currents, the material gain at different current densities and wavelengths were deduced by using Eq (1). A standard mode solver was also used to calculate the optical confinements and

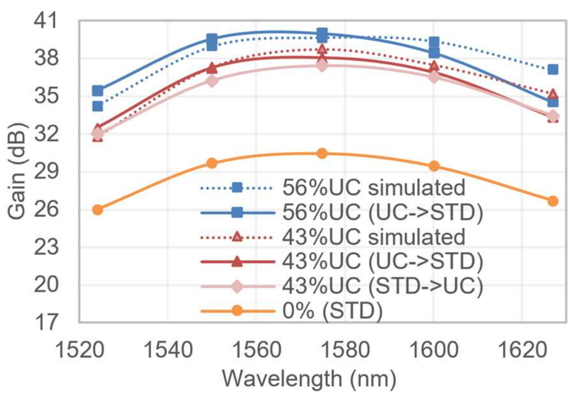

Fig. 3: Small-signal Gain spectrum for 3 types of 4mm chips (56% upper cladding part, 43% upper-cladding part and standard one) with -25 dBm input power and 1.3 A biased current: "UC→STD" with optical signal injected from upper-cladding side. Plain lines are measured spectra, dashed lines are simulated spectra.

propagation losses. Thus, we were able to predict the gain spectrum for each upper-cladding design which was plotted with a dashed line in Fig. 3. The agreement between the simulated and measured results was found within 1dB except at long wavelengths.

In Fig. 4, the measured chip gain at 1600 nm as a function of the chip output power is shown for the different devices. The chip P_{sat}, corresponding to the output power at which the amplifier gain is reduced to half of the small signal gain (-3 dB), is deduced for each device. Again, the 43% UC device was measured from each input. The markers on the Chip Pout axis of Fig. 4 represent the chip saturation output power of each device.

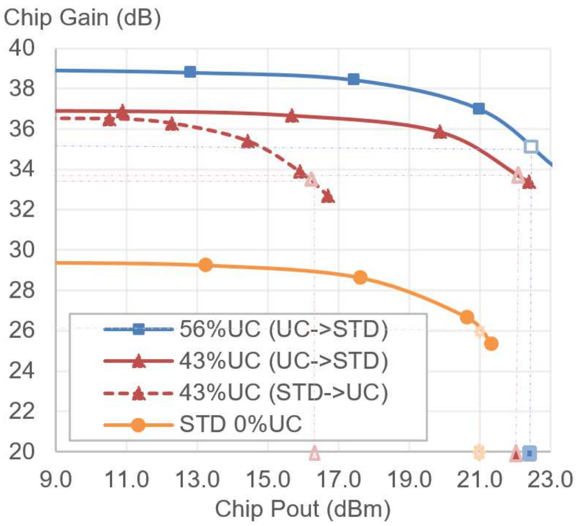

Fig. 4: Gain vs Pout at 1600 nm. The markers on the axis Pout represent the saturation output power of each device.

The chip saturation output power with standard section at the output is around 22 dBm with either UC chips which is about 1 dB higher than the standard chips P_{sat}. This is due to a stronger current density caused by a smaller total active volume induced by the narrow ridge in the upper-cladding section, and consequently a smaller differential gain. With the UC section at the output, the measured P_{sat} would be the saturation output power of the UC section, much smaller than the standard one, which is close to what we calculated: 16dBm.

These results validate this novel dual-stage design to achieve simultaneously high gain and high saturation output power at a moderate bias current.

Calculations of $G_0 x P_{sat}$ product

The G_0 x P_{sat} product is a figure of merit showing the trade-off between P_{sat} and chip gain to be evaluated in terms of material and device parameters [3]. After converting all the parameters to standard units, the tested devices values of G_0 x P_{sat}, in W, are compared with other reference designs [1] [2] as shown in Fig.5. Due to its large gain (~40dB) and high P_{sat} (22 dBm) at 1600 nm, the 56% upper-cladding SOA design is at the leading position by a factor of 10, 220 and 68 respectively in comparison to the standard design, references [1] and [2] respectively.

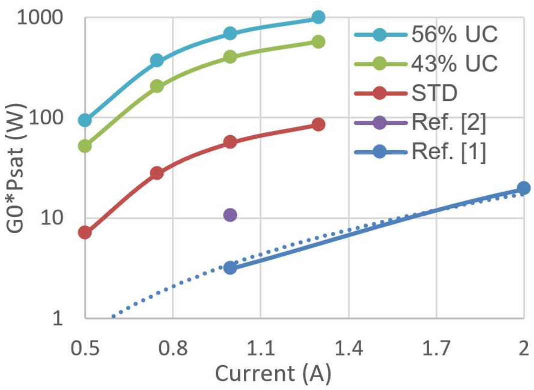

Fig. 5: G_0 x P_{sat} product

Conclusions

A novel SOA design was presented based on a dual-section design in order to mitigate the usual trade-off between gain and saturation output power. Indeed, by introducing an upper-cladding over a portion of the chip length hence creating a dual section, high gain (up to 40 dB) and high saturation optical power (22 dBm) were measured and subsequently, the best G_0 x P_{sat} trade-off was achieved in comparison to the state of the art.

Future work will include the fine tuning of the UC section design length and the optimization of the transition taper.

References

[1] P. W. Juodawlkis et al, "Packaged 1.5-um Quantum-Well SOA With 0.8-W Output Power and 5.5-dB Noise Figure", *IEEE Photon. Technol. Lett.*, vol. 21, no. 17, pp. 1208–1210, Sept. 2009

[2] K. Morito, S. Tanaka, S. Tomabechi, and A. Kuramata, "A broad-band MQW semiconductor optical amplifier with high saturation output power and low noise figure," *IEEE Photon. Technol. Lett.*, vol. 17, no 5, pp. 974–976, May 2005.

[3] P. W. Juodawlkis and J. J. Plant, "Gain-power trade-off in low-confinement semiconductor optical amplifiers," in *Proceedings of the International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD)*, 2007.

[4] A. Verdier *et al*, "Ultrawideband wavelength-tunable hybrid external-cavity lasers," *Journal of Lightwave Technology*, vol. 36, no. 1, pp. 37–43, 2018.

[5] H. Carrere, V. G. Truong, X. Marie, R. Brenot, G. De Valicourt, F. Lelarge `and T. Amand, "Large optical bandwidth and polarization insensitive semiconductor optical amplifiers using strained InGaAsP quantum wells," *Appl. Phys. Lett.,* vol. 97, 2010, Art. no. 121101.