8x 2Gb/s LED-Based Optical Link at 420nm for Chip-to-Chip Applications

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Abstract Using an array of 8 high-speed GaN-based emitters on sapphire, together with a custom lateral p-i-n Si CMOS detector array and discrete electronics, we demonstrate an aggregate 16Gb/s in a rectangular multicore imaging fiber <0.2mm on a side.

Introduction

Data connections between silicon ICs are a bottleneck for the industry. Today, nearly all short distance interconnects are electrical, with limited density and high-power consumption due to the intrinsic capacitance and resistance of wires. For decades, short optical interconnects have been investigated but the requirements of wide operating temperature, low drive power, and compatibility with silicon electronics have proved challenging.

The display industry has developed the technology to fabricate millions of micron-sized GaN LEDs and transfer them to silicon backplanes with high yields. We have developed GaN emitters optimized for high-speed modulation that we call CROMEs – Cavity Reinforced Optical Micro-Emitters. These devices are fully compatible with the display manufacturing ecosystem.

On the receiver side, detectors are straightforward, given the short absorption length of blue light in silicon. Here, we describe a lateral CMOS-compatible lateral p-i-n detector that has high quantum efficiency and very low capacitance per unit area.

Light from a 2D array of optical transmitters can be coupled to a 2D array of optical receivers using an “imaging fiber” consisting of thousands of cores, each typically < 10um in diameter. The imaging fiber can replicate the optical distribution on its input face at its output face. The light from each transmitter can be carried in a single core, or through a number of smaller cores. In all cases, we consider only very highly multimoded fibers with typical size of the beam in the tens of microns. This allows loose alignment packaging and is adequate for the short distances considered.

In contrast to previously-reported LED links in single core step-index plastic fibers[1], we demonstrate higher speeds per lane and use spatial division multiplexing[2] to achieve a larger number of lanes with simple on-off modulation format, to reach a record aggregate bandwidth.

Components

The CROMEs were grown on a patterned sapphire substrate with custom epitaxy that optimizes carrier lifetime without compromising too much on quantum efficiency (QE). Each CROME had separate contacts with parasitic capacitance minimized. The characteristics of these devices have been reported previously, with NRZ links up at multigigabit rates[3]. Though we are leveraging insights from previous work done for Li-Fi applications[4], where nominally a lighting LED is used for data transmission, the CROMEs are much faster, as we are able to optimize the epitaxy and device structure while trading off some QE for speed. We estimate the CROMEs to have an internal QE of about 20% and these particular devices had an external QE of about 3%. This can be improved with encapsulation to reduce total internal reflection (TIR), microlens/optical collector structures, and by transferring the CROMEs onto a substrate with a back reflector. A top view of the CROME

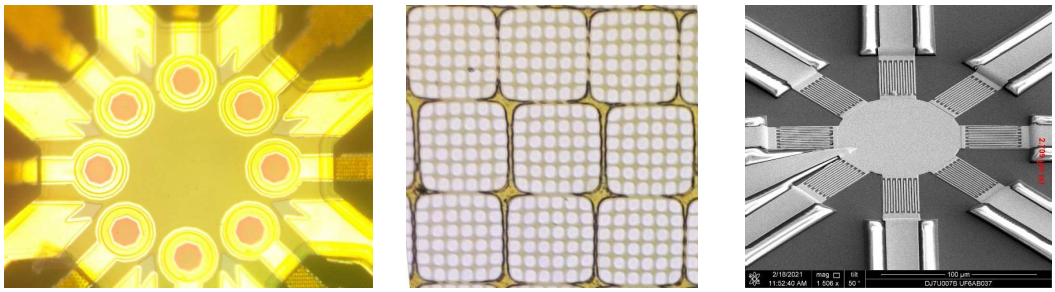

Fig. 1: Components for the link. Left: 8 element emitter array. Center: imaging fiber consisting of 9 elements of 6x6 with 10μm cores – note each lane is carried by a few adjacent cores. Right, 8 element lateral p-i-n detector array

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array is shown in the left-most picture of Fig 1. Each device has a mesa width of about 30µm with an output aperture of about 25µm. The eight devices were equally spaced on a circle of diameter 130µm.

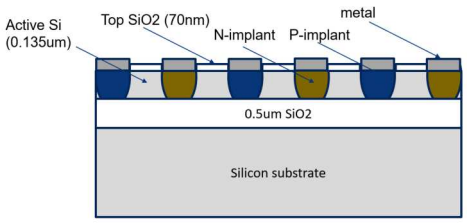

Fig. 2: Lateral p-i-n detector

The detectors were lateral p-i-n structures fabricated on a silicon-on-insulator (SOI) wafer. The process sequence was modelled on a commercial XFAB 130nm CMOS process to demonstrate photodiode compatibility with standard commercial CMOS processes. (photo on the right of Fig. 1; lateral cross-section diagram in Fig. 2). The n and p junctions were similar to the source and drain of the CMOS FETs and we used the same lightly doped base wafer.

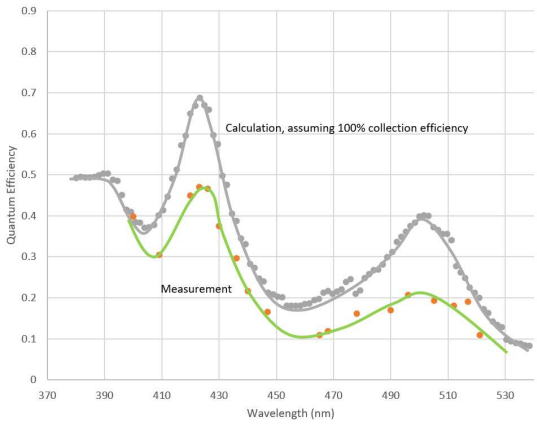

Fig. 3: Measured QE of detectors versus calculation

The detectors had a maximum efficiency value of about 0.16A/W for devices with minimal shadowing, or roughly 50% QE at 420nm. Fig. 3 shows the calculated and the measured QE as a function of wavelength. The theoretical calculation was done using the matrix multiplication method, taking into account the real and imaginary refractive indices of the materials, with a slight adjustment of the cavity thickness to fit the same peak position as the data. It assumes that all the absorbed light in the thin silicon device layer is converted to photocurrent. The measurement was done with a white light source and a monochromator, and shows a peak efficiency about 30% lower than the theoretical prediction. This is mostly likely due to errors in the thickness of the top oxide which acts as an anti-reflection coating, and due to carrier recombination at the Si/SiO_2 interface. The buried oxide acts a reflector, giving a resonance peak at the desired wavelength. The overall efficiency is limited by the absorption in the very thin 0.135µm active device and could be improved by a thicker device layer or with an optimized back reflector.

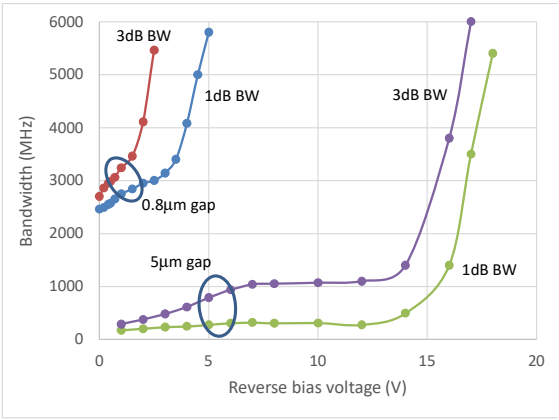

Fig. 4: Bandwidth of lateral p-i-n detectors as a function of reverse bias voltage.

Devices were fabricated with various gaps betwen the n and p fingers, and the high frequency characteristics measured with a 6GHz network analyzer. The 1dB and 3dB fall off frequencies are plotted in Fig. 4 as a function of reverse bias voltage. The narrowest gap device at about 0.8µm had a 3dB bandwidth of 6GHz at about 2V reverse bias, while the longer 5µm gap was at about 17 volts.

One advantage of these lateral structures is the extremely low capacitance per unit area, allowing bigger devices and therefore looser tolerances in packaging. We estimate the capacitance of a 30 µm diameter detector with the 2µm fingers and 5µm gap to be about 10fF. The capacitance of larger devices of about 60µm diameter was measured directly and was below 100fF, limited by the resolution of the setup. Our speed results are comparable to previous work[5], but we show a higher efficiency, presumably due to the better Si/SiO_2 interface and superior material quality.

The detectors were then packaged with 8 commercial Hilight TIA die with about 2GHz bandwidth mounted directly on the surface of the detector, as shown in Fig. 5.

The fiber bundle uses imaging fiber supplied by Schott. The particular fiber bundle was a 3x3 grid of a multicore structure, each of which was a 6x6 rectangular array of 8µm cores spaced at

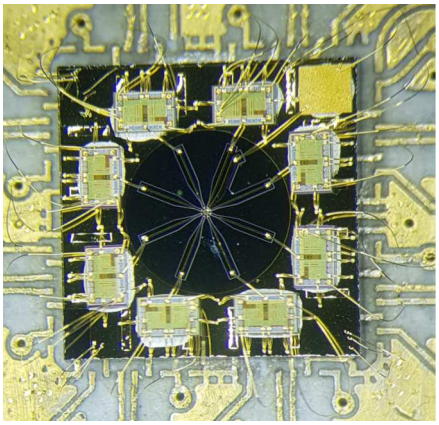

Fig. 5: The TIAs were mounted directly on the detector chip.

10µm, with an NA of 0.6. The relative positioning of the fiber cores was relatively accurate, as each 36 element fiber was pulled simultaneously. However, there is some irregularity of the 3x3 epoxied assembly, as shown in the center picture of Fig. 1. Given the 25µm aperture of each CROME, the light in each channel was generally carried by a few cores. There was some variation depending on whether the CROMEs lined up with the irregular gaps, causing up to 1dB change in the received power. Each sub-bundle was approximately 60µm on a side, and the entire 3x3 assembly was about 180µm on a side and a length of about 60cm.

Link

The 8 channel link was completed by butt-coupling the fiber between the emitter and detector arrays and adjusting the rotation such that each emitter was connected to its respective detector. A alignment tolerance of a few microns was enabled by the relatively large detectors. Detectors with 5µm gaps between fingers were used, with an external bias to increase the speed. The emitters were driven at a current of about 10mA and about 40µW was received at each detector. The bandwidth was limited by the TIAs and the instrumentation to 2Gb/s per channel. To measure the BER, a Xilinx VC707 FPGA evaluation board with 8 GTX transceivers was programmed to generate independent 2Gb/s pseudo-random on-off bit sequences and count errors. However, we could only simultaneously measure the BER of 5 channels due to issues with the GTX receiver. Fig.6 shows the BER curves of the channels at this speed both individually and when all were driven simultaneously with about 1dB measurable crosstalk.

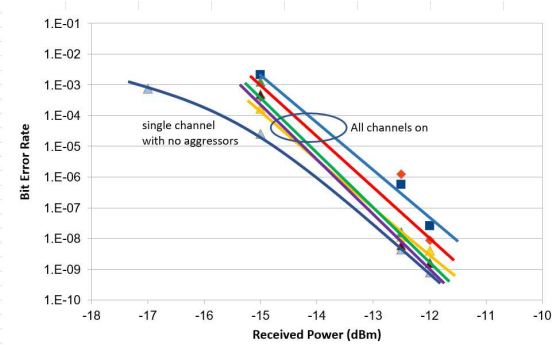

Fig. 6: BER of the channels, typical with no other channels on, and also measurement of 5 of the 8 carrying data simultaneously.

Conclusions

Though the link is far from optimized, we demonstrated record aggregate bandwidth and density of an LED-based interconnect. With 2Gb/s on-off modulation per lane in a thin multicore fiber assembly, we show 16Gb/s total bandwidth and a density of 0.5Tb/s per square millimeter. The per-channel speed can be extrapolated from other work to 10Gb/s, while the number of channels with suitable packaging can scale to hundreds per square mm. Optimized collectors, coupling, and higher-speed matched TIAs can tremendously improve the performance of these links. All the technologies demonstrated can be readily integrated on silicon, including drivers, detectors, and high sensitivity TIAs for future high-bandwidth chip to chip communications.

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