

High-speed IM/DD transmission with analog (de-)multiplexers

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Abstract In this paper we give an overview on the status of devices for analog multiplexing and demultiplexing and experimental results in general and on the results achieved within the ECSEL Taranto project.

Introduction

Today's coherent optical transponders are applying digital-to-analog converters (DAC) in the transmitter and analog-to-digital converters (ADC) in the receiver along with digital signal processing (DSP). For commercial transponders these devices are manufactured in CMOS technology and monolithically integrated with the respective DSP part. Despite the huge technological progress in CMOS manufacturing over the last years at one point it will be difficult to fulfil future requirements on resolution, analog bandwidth and sampling rate.

Analog signal processing has the potential to reduce the requirements for CMOS DACs and ADCs at the cost of parallelization. In this paper we focus on time-domain analog signal processing.

Analog Multiplexing

At the transmitter side, an extension of the analog bandwidths and sampling rate can be achieved using analog multiplexers^[1-6] (AMUX), which take parallel data signals at lower speeds and interleave them to form high-speed signals. Reported performances of spectral efficiency (SE) versus the net data rate for optical back-to-back (B2B) are summarized in Fig. 1. They are calculated for a single modulation dimension.

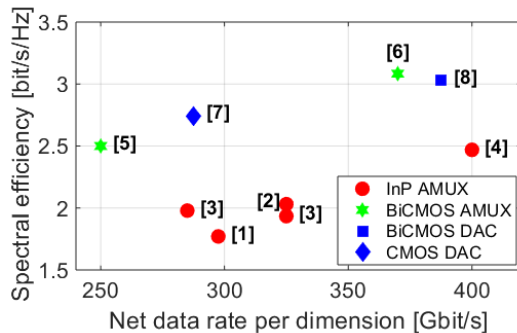


Fig. 1: Summary of reported AMUX and DAC Net data rates

In^[1-4] InP based AMUXs were applied and despite of achieving a high net data rate of up to 400 Gbit/s, the SE was limited to ~2.5 bit/s/Hz^[4]. The use of a BiCMOS AMUX^[5,6] allows for operation at higher SE >3 bit/s/Hz^[6]. The comparison with CMOS and BiCMOS DACs^[7,8] shows that the BiCMOS AMUX outperforms CMOS DACs^[7] and is on par with the BiCMOS DAC^[8].

The 2:1 BiCMOS AMUX used in our experiments^[5,6] was developed in the Taranto project. It is a prototype working up to 120 GSa/s and was designed by Saarland University, more detail on the device can be found in^[9]. It was fabricated by STMicroelectronics in their 55 nm BiCMOS technology. The module, the electrical frequency response including the two DACs and electrical eye diagrams at 120 GBaud are shown in Fig. 2.

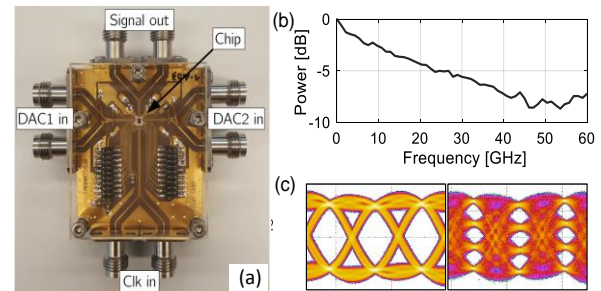


Fig. 2: (a) AMUX module, (b) Joint frequency response of AMUX and two DACs. and (c) electrical eye diagrams at 120 GBd

Fig. 3 shows the schematic setup of an AMUX based transmitter. In general, the AMUX is driven by two DACs and a half-rate clock. Its electrical output signal is amplified, and it is modulated by a Mach-Zehnder modulator.

In a first experiment^[5] the AMUX was operated at 100 GSa/s for 100 GBd short reach PAM-4, -6 and -8 transmission.

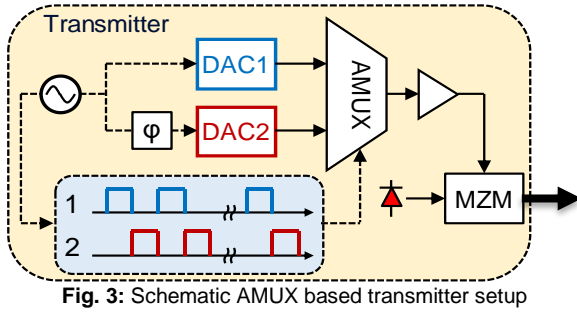


Fig. 3: Schematic AMUX based transmitter setup

The transmission link consisted of 5 to 20 km of SSMF followed by a Bragg-grating based tuneable dispersion compensator. For receiving the optical signal an SOA pre-amplified 100 GHz photodiode and a real-time oscilloscope (RTO) with 84 GHz bandwidth and 256 GSa/s were applied. We stored the received data on a PC and in an offline DSP we resampled the data and after an adaptive decision-directed FIR filter the Bit error ratio is calculated.

After 20 km SSMF transmission we achieved net data rates of 189 Gbit/s for PAM-4, 233 Gbit/s for PAM-6 and 250 Gbit/s for PAM-8 modulation. The BER versus the transmission distance and the BER versus the received power are shown in Fig. 4.

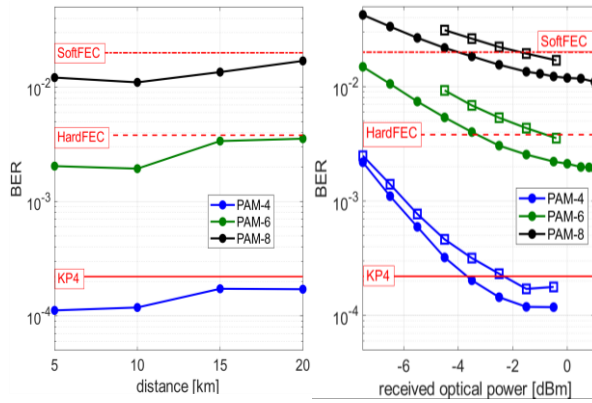


Fig. 4: left: BER vs. transmission distance, right: BER vs. received power for 10km (circles) and 20km (squares)

We also worked with the AMUX at its maximum sampling rate of 120 GSa/s [6]. The transmitted signal consisted of 4 digital sub-carriers at 14.4 GBd, each carrying a PCS 256QAM, with RRC pulse shaping.

The black curve in Fig. 5 (a) (Pre-emph A) shows the digital pre-emphasis including all transmitter components. We also varied the pre-emphasis per subcarrier in steps of 1 dB together with the entropy of the PCS to maximize the overall data rate. The optimum pre-emphasis was found to be a stepwise reduction of 1 dB towards the outer subcarriers (Pre-emph B) and the resulting optical spectra are displayed in Fig. 5 (b).

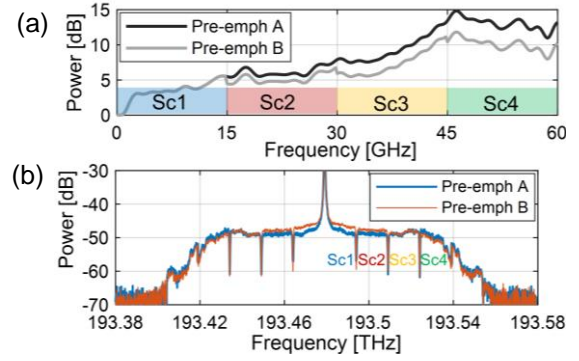


Fig. 5: (a) The two different pre emphasis schemes. (b) Resulting optical spectra

In back-to-back we observed an average gain over all subcarriers of ~ 0.25 bit/symbol for Pre-emph. B resulting in an average Net information rate of 6.44 bit/symbol and a combined net data rate of 370 Gbit/s.

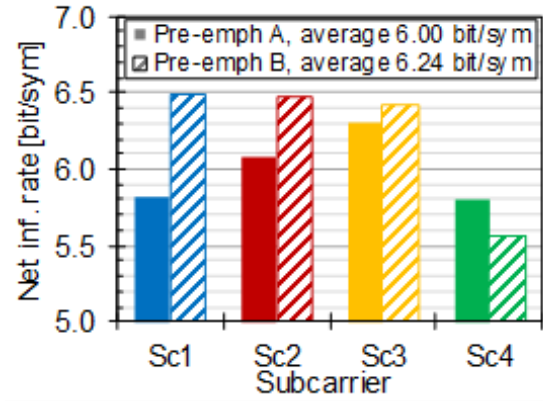


Fig. 6: Net information rates on 4 subcarriers after 10 km of fiber transmission

In Fig. 6 the net information rate is shown on each subcarrier after transmission over 10 km SSMF + DCF. The average net information rate is 6.00 bit/sym with Pre emph A and increases to 6.24 bit/sym with Pre emph B. Combined net data rates of 346 Gbit/s and 360 Gbit/s are achieved with Pre-emph A and Pre-emph B, respectively.

Analog Demultiplexing

At the receiver side, a reduction of the analog bandwidths and sampling rates of the ADCs can be achieved by analog demultiplexing [10-12] (ADMUX), which parallelize the incoming high-speed signals data signals into lower speed analog signals. These can then be A/D converted by lower speed ADCs. To our best knowledge the devices in [10,11] have not been applied in optical experiments to date.

The 1:4 ADMUX used in our experiments [12] is based on a charge-sampling architecture and all inputs and outputs are differential. It was fabricated in 130 nm SiGe BiCMOS technology from IHP (SG13G2) and can be operated up to

112 GSa/s when connecting to a half-rate clock, see [12,13] for further details.

The schematic ADMUX based receiver setup used in our experiments is shown in Fig. 7. A high-speed photodiode does the o/e conversion and is followed by an electrical amplifier to provide sufficient input swing to the ADMUX. The ADMUX demultiplexes the incoming signal into four parallel 28 GSa/s data streams. As the outputs must be operated differentially, a quad-differential-to-single ended amplifier is inserted before the signals are quantized by the RTO, in this case one working at 50 GSa/s and a bandwidth adjustable from 14-20GHz and stored on a computer for offline DSP.

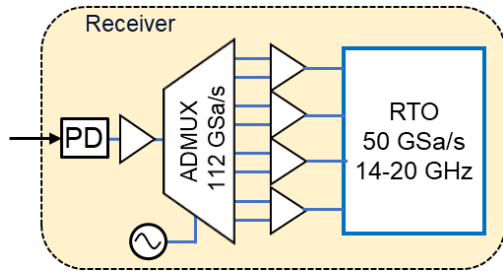


Fig. 7: Schematic ADMUX based receiver setup

We performed a 100 GBaud PAM 4 short reach transmission experiment [14] over SSMF with the above described ADMUX based receiver setup, the different link configurations can be seen in Fig. 8.

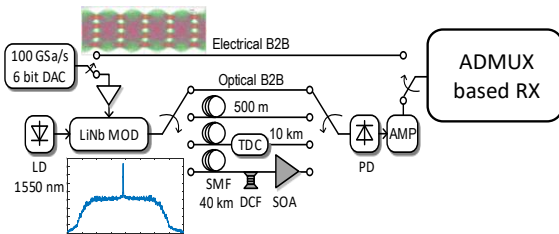


Fig. 8: Schematic experimental setup for short reach PAM 4 transmission

As the sampling rate of the ADMUX is asynchronous to the transmitter and the RTO, in the offline DSP the original signal had to be reconstructed.

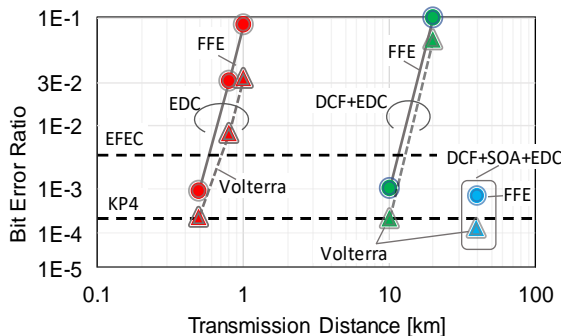


Fig. 9: BER vs. distance for the different link lengths

First this was done data-aided and in a later work a blind algorithm was presented [15]. In Fig. 9 the results for the different link configurations are summarized together with the different equalization schemes in the DSP, namely feed-forward and Volterra equalizer. We show the results without optical dispersion compensation (red symbols), with tuneable dispersion compensator (green symbols) and with DCF (blue symbols), respectively.

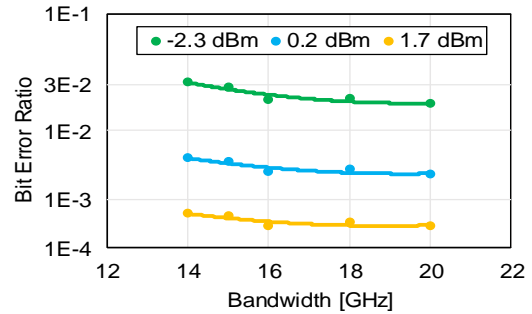


Fig. 10: BER vs. RTO bandwidth at different received optical power

In Fig. 10 the results for varying the RTO's bandwidth applying a built-in brickwall filter are given at different received optical power for the bottom configuration in Fig. 8. As long as the RTO bandwidth amounts 16 GHz or more there is no significant change of the BER, only towards lower bandwidth a penalty is observed.

Conclusions

In this paper we gave an overview on the status of analog multiplexing and demultiplexing. As examples we also present the experimental results achieved in our Lab for short reach IM/DD transmission with an AMUX at 100 and 120 GSa/s and an ADMUX for receiving 100 GBaud at 112 GSa/s, both devices made in BiCMOS.

Acknowledgements

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References

- [1] F. Hamaoka, et al., "144-Gbaud PDM-32QAM and 168-Gbaud PDM-16QAM signal generation ...," in Proc. ECOC 2019, pap. Tu3B.1.
- [2] N.-P. Diamantopoulos, et al., "Net 321.24-Gb/s IMDD transmission based on a >100-GHz bandwidth ...," in Proc. OFC 2020, pap. Th4C.1
- [3] M. Nakamura, et al., "1.3-Tbps/carrier net-rate signal transmission with 168-Gbaud PDM PS-64QAM ...," in Proc. ECOC 2019, pap. Tu2D.5
- [4] H. Yamazaki, et al., "Net-400-Gbps PS-PAM

transmission using integrated AMUX-MZM," *Opt. Express* 27(18), 25544-25550 (2019).

- [5] K. Schuh, et al., "100 GSa/s BiCMOS analog multiplexer based 100 GBd PAM transmission ...," in *Proc. ECOC 2020*, pap. Tu1E.2
- [6] Q. Hu, et al., "120 GSa/s BiCMOS Analog Multiplexer Enabling 360 Gbit/s DSCM PCS 256QAM IM/DD Transmission", in *Proc. OFC 2021*, paper F2D1
- [7] F. Buchali et al., "1.1 Tb/s/lambda at 9.8 bit/s/Hz DWDM transmission over DCI distances ...," in *Proc. OFC 2020*, pap. Th3E.2
- [8] F. Buchali et al., "1.52 Tb/s single carrier transmission supported by a 128 GSa/s SiGe DAC," in *Proc. OFC 2020*, pap. Th4C.2
- [9] M. Collisi, M. Möller, "A 120 GS/s 2:1 analog multiplexer with high linearity in SiGe-BiCMOS technology," in *Proc. 2020 BCICTS*, pap. 4a.2.
- [10] K. Vasilakopoulos, et al., "A 108GS/s track and hold amplifier with MOS-HBT switch," 2016 IEEE MTT-S International Microwave Symposium (IMS), San Francisco, CA, 2016, pp. 1-4.
- [11] A. Zandieh, et al., "128-GS/s ADC Front-End with Over 60-GHz Input Bandwidth in 22-nm Si/SiGe FDSOI CMOS," 2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), San Diego, CA, 2018, pp. 271-274.
- [12] X. Du et al., "A 112-GS/s 1-to-4 ADC front-end with more than 35-dBc SFDR and 28-dB SNDR up to 43-GHz in 130-nm SiGe BiCMOS," 2019 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Boston, MA, 2019, pp. 1-4.
- [13] F. Buchali, et al., "A SiGe HBT BiCMOS 1-to-4 ADC Frontend Enabling Low Bandwidth Digitization of 100 GBaud PAM4 Data," in *Journal of Lightwave Technology*, vol. 38, no. 1, pp. 150-158, 1 Jan.1, 2020, doi: 10.1109/JLT.2019.2951592
- [14] F. Buchali, et al., "A SiGe HBT BiCMOS 1-to-4 ADC Frontend Supporting 100 GBaud PAM4 Reception at 14 GHz Digitizer Bandwidth," 2019 Optical Fiber Communications Conference and Exhibition (OFC), San Diego, CA, USA, 2019, pp. 1-3.
- [15] F. Buchali, et al., "SYSTEM IMPLEMENTATION OF A 112 GSA/S 1-TO-4 ADC FRONTEND FOR 100 GBAUD PAM4 RECEPTION", in *Proc. ECOC 2019*, pap. Tu.2.D3