Novel Precise Time Synchronization and Distribution for Multilayer Optical Metro and Access Networks

Bitao Pan, Xuwei Xue, Fulong Yan, Xiaotao Guo, Nicola Calabretta

Institute of Photonic Integration, Eindhoven University of Technology, Eindhoven, the Netherlands, b.pan@tue.nl

Abstract We present and experimentally assess a novel time slotted optical metro access network with precise time distribution and nodes synchronization. Results confirm successful time-slotted metro network operation with 5ns time accuracy and <12ns in two-layer metro and 5G fronthaul network with a single time reference.

Introduction

5G fronthaul networks will need to serve latency critical traffic like enhanced Common Public Radio Interface (eCPRI) based base band units (BBUs) and remote radio units (RRUs) communications. This type of communication requires accurate time synchronization for achieving ultra-low latency jitter. In addition, new network services such as high accuracy positioning, industrial 4.0 and new 5G technologies like the carrier aggregation (CA) and joint transmission (JT) demand ultra-high time accuracy. 5G and beyond 5G network is expected to realize ultra-high connection density and mobility, which introduce more stringent requirements on time synchronization [1, 2]. Considering the large number of 5G RRUs, deploying many Global Navigation Satellite System (GNSS) for all the RRUs and BBU nodes is very heavy to maintain and very expensive. Therefore, to bring accurate time synchronization to the network and avoid the high cost from deploying many GNSS, precise time distribution over optical network needs to be investigated. There are existing technologies [3, 4] for time synchronization between two network nodes based on timestamp exchange. However, these technologies face the issue of time offset accumulation in case that they are used for synchronizing many cascaded nodes. For instance, a slave node is used as the time reference for another slave node in the cascaded point to point time distribution system. It introduces accumulated time offset between time reference node and cascaded slave nodes.

To address the mentioned issue, we propose and experimentally demonstrated a novel control and synchronization mechanism in time-slotted optical metro access networks for precise time synchronization. We introduce a dedicated supervisory channel and protocol that enable time-slotted operation of the network by carrying the timestamp of each node for timestamp exchange and reference time distribution to the network nodes. In addition, the supervisory channel is also carrying the destinations of the WDM data channels in each time slot to enable fast add/drop control and wavelength reusing as well as time slot reservation for protected traffic. The precise time distribution and synchronization mechanism presented in this work can prevent the time offset accumulation issue for large networks with many cascaded nodes. The nanoseconds control and synchronization of the network have been experimentally verified by an FPGA-based implementation of the proposed protocol. The results show below 5ns time accuracy for all the metro ring network nodes, and <12ns time accuracy has been achieved for extended metro ring and 5G fronthaul network with a single time reference.

Precise Time Distribution and Sychronization Based Metro Access Network Operation

The schematic of the proposed fast optical add drop multiplexer (fOADM) based optical metro access ring network with precise time distribution and synchronization is shown in Fig. 1(a). The fOADM enabled metro access network operates in a time slotted way, and under the control of a dedicated out-of-band supervisory channel and protocol. The supervisory channel carries the label information of the WDM data channels (and the available wavelength) in a control packet for each time-slot to address the node destinations, avoiding static wavelength allocation to address a certain node. Each control packet includes a packet preamble, a timestamp and destination data, which is formatted as an array of bit sequences. Each bit sequence represents the destinations of a related wavelength (lambda). If a wavelength channel needs to be dropped to the i-th node, then the related i-th bit in the sequence is set to 1, otherwise to 0. The control of the node modifies the supervisory channel according to the dropped and added wavelengths, and then sends it out the updated information to the next node. The other key function of the supervisory channel is precise time distribution over the network. As



Fig. 1: (a) Architecture of the time slotted optical ring network with precise time distribution; (b) Mechanism of the proposed precise time distribution without offset accumulation; (c) time stamp exchange between master and slave nodes.

shown in an example in Fig. 1(b), the timestamp of n-th node is carried by the control packet in the supervisory channel in the n-th time slot. All the timestamps of the slave nodes are only exchanged with the master node for time synchronization, and each time slot is dedicated for the synchronization between the master and one of the slaves. In the initialization of the time distribution process, the master node first adds its local time (TM-n(1)... TM-n(2)) into the control packets of the related time slots. The n-th slave node detects the n-th time slot, then receives the master timestamp TM-n(1), records the receiving time TS-n(1) and adds its own time TS-n(2) to the control packet. When the control packet of the nth time slot is back to the master node, the master node records the receiving time TM-n(2), and adds TM-n(2) to the control packet. After the n-th slave node receives the TM-n(2), the node knows all the 4 timestamps as shown in Fig. 1(c). By using equation (1) and (2), the algorithm proposed in IEEE1588 [3], the n-th slave node can calculate its time offset to the master node and adjusts its local timer. The advantage of this mechanism is that all the slave nodes can directly synchronize their time with the master node rather than cascaded point to point time distribution, avoiding the accumulated time offset. In addition, the control packets and the label information carried by the supervisory channel are continuously running for the full network management and operation, so the time sychronzation is continuously updated.

$$delay = \frac{(T_{S-n(1)} - T_{M-n(1)}) + (T_{M-n(2)} - T_{S-n(2)})}{2}$$
(1)

$$offset = \frac{(T_{S-n(1)} - T_{M-n(1)}) - (T_{M-n(2)} - T_{S-n(2)})}{2}$$
(2)

Experiment Setup and Results

The experiment setup to assess the proposed network is shown in Fig. 2(a). It is composed by a ring network with three fOADM nodes connected by 25, 10 and 2.8Km fibers. Each fOADM is equipped with a SOA-based wavelength blocker (WBL) module for fast wavelength add/drop and a Xilinx UltraScale FPGA board for time synchronization, optical components control and traffic engineering. SFP+ modules are employed for implementing the data channels and supervisory channel. The 10GE PCS/PMA is employed as the physical layer of the supervisory channel for the data (de)coding and RX Byte alignment. 2us time slot is implemented in the experiments with 150ns guard time between data packet and control packet to account the processing of the control packets and the setting of optical add drop components. Node 1 (master node) is used to provide the reference time to the optical network by its local clock running at 250MHz. An FPGA based sub-node, emulating the access clients that require time synchronization like 5G antennas and baseband units, is connected to the node 2 (slave) by a 10GE link for investigating the time synchronization over multiple layers of the optical network to its access clients. The node 2 acts as time reference of the sub-node.

First, the time slotted operation is verified. Fig.2(b) shows the recorded trace of the received supervisory channel at node 1 in each time slot after multiple runs in the FPGA controlled time slotted optical ring network. It indicates that the control packets inside the supervisory channel are operated in correct time slot with accurate



Fig. 2: (a) Experiment setup; (b) FPGA trace of the supervisory channel and received time stamp of master node; (c) gap between two PPS signal of master node and node 2; (d) Histogram of the time offset between master node and node 2; (e) Histogram of the time offset between master node and sub node.

timing. Note that the control packets in the supervisory channel are packaged in XGMII format, which contains data (64 bits) and control flags (8 bits). The idle data ("Ox07" in Fig.2(b)) in the supervisory channel is to make the supervisory channel can continuously send and receive data between nodes for clock distribution and retrieving. Dynamic time slotted wavelength add/drop operation is also shown in the figure, where the node destinations of the wavelength channels are encoded in 3 bits data addressing at which node the wavelength channels should be dropped. This information processed by the FPGA based control of each node is used to properly turning on and off the SOA gates of the WBL. Fig. 2(b) also shows the received time stamp inside one time slot of node 1. The time stamps consist of 32bits in nanosecond domain and 48 bits in seconds domain. Note that the time accuracy in the second domain has been measured via the ILA core of Xilinx Vivado [5] by manually triggering two boards at the same time. The time offset in nanosecond domain has been measured by an oscilloscope that is connected with the FPGAs. Each FPGA node generates a pulse per second (PPS) signal according to its clock. By measuring the gap between two pulses from two nodes, the time offset can be measured. Fig 2.(c) shows the PPS signal of the master node and node2 in one measurement, the zoom in picture illustrates an around 3.5ns time offset. Fig. 2 (d) and (e) show the time offset statistic of node 2 and node 3 in 200 measurements. The two nodes have similar time offset performance

because the master can directly exchange timestamps with all the slaves in the ring network. There is no accumulated time offset in the ring, which is not avoidable in the cascaded point to point time distribution system. The time offset is distributed in two peaks spaced by 4ns because the timer in the FPGAs is running at 250MHz (granularity and phase uncertainty is 4ns). Therefore, when the slave nodes calculate time offset and delay, the phase difference is mostly counted as 0 or 4 ns. Fig. 2(f) shows the time offset between the master node and the sub node. It can be seen that the time offset is mainly distributed at 4ns. and most of the offsets are below 10ns, which is acceptable for the most stringent synchronization requirements of 5G [1]. It indicates that the proposed time distribution and synchronization method can be used in a two-layer optical metro access network with only one GNSS for the master node to distribute the time with <12ns accuracy.

Conclusions

We have experimentally demonstrated a fast controlled time slotted optical network with precise time distribution by a novel supervisory channel control. Below 5ns time accuracy for all the ring network nodes has been achieved. Less than 12ns time synchronization accuracy has been achieved in the ring network and its access nodes with a single time reference, which is acceptable for the most stringent requirements of 5G fronthaul networks.

References

- [1] Li H, Han L, Duan R, et al. Analysis of the synchronization requirements of 5G and corresponding solutions[J]. IEEE Communications Standards Magazine, 2017, 1(1): 52-58.
- Parvez I, Rahmati A, Guvenc I, et al. A survey on low [2] latency towards 5G: RAN, core network and caching solutions[J]. IEEE Communications Surveys & Tutorials, 2018, 20(4): 3098-3130.
- [3] IEEE 1588 standard, online available:
- <u>https://standards.ieee.org/standard/1588-2008.html</u>.
 [4] Lipiński, M., Włostowski, T., Serrano, J., & Alvarez, P. (2011, September). White rabbit: A PTP application for robust sub-nanosecond synchronization. In 2011 IEEE International Symposium on Precision Clock Synchronization for Measurement, Control and Communication (pp. 25-30). IEEE. [5] Xilinx LogiCORE IP Product Guide, online available:
- https://www.xilinx.com/support/documentation/ip_doc umentation/ila/v6_2/pg172-ila.pdf