Robust Topology Optimization for Foundry-Photonics Inverse Design: Examining Compact and Arbitrary Power Splitters

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Abstract We present a novel framework for robust inverse-design of semiconductor-foundry devices tolerant to standard fabrication variability. We designed and tested compact 50/50, 90/10, and 99/1 power splitters sampled across multiple wafers on a commercial silicon photonic process, demonstrating $< \pm 2\%$ deviation over 100 nm of bandwidth.

Introduction

Recent advances in large-scale photonic integration, particularly on commercial foundry platforms, continue to enable the next generation of both classical and quantum telecommunications applications[1]. As is the case with standard electronic CMOS processes, integrated photonic foundry platforms deploy process development kits (PDK) qualified for a prescribed manufacturing tolerance and performance variation, thereby providing a comprehensive framework needed to design complicated systems on a large scale[2]. Unfortunately, even fundamental system blocks like power splitters and directional couplers exhibit a large variation in splitting ratio, insertion loss, and phase accumulation[3], which either restricts the range of applications or forces designers to dynamically tune their systems after fabrication[4], a costly compromise.

We present a novel robust design framework using density-based topology optimization (TO) adapted specifically for large-scale commercial foundries. We validate our framework by designing and experimentally testing three compact ($3\mu m \times 3\mu m$), power splitters with precise 50/50, 90/10 and 99/1 split ratios. Each device was fabricated on the GLOBALFOUNDRIES 9WG, 300 mm silicon photonics process[5]. Experimental tests for each splitter over three devices randomly sampled across three different wafers reveal remarkably consistent splitting ratios for both outputs ($\pm 2\%$ for the 90/10 case) over 100 nm of bandwidth. We build upon previous work that designed arbitrary splitters using analytic adiabatic methods[6],[7], particle-swarm algorithms[8], deep learning[9] and even other TO methods[10], noting that our approach is the first to produce designs that obey standard foundry design rule checks (DRC)[2], are explicitly broadband, and demonstrate robustness to common sources of manufacturing variability, namely over/under-etching[11]. Our methodology can design devices far more complex than power splitters, and we anticipate its use in designing next-generation PDK components for highly sensitive applications.

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Device design

Our robust design framework parameterizes the device at every "pixel", continuously evolving millions of degrees of freedom using standard gradient-descent algorithms[12],[13]. By leveraging an adjoint-variable method[14], we efficiently calculate the gradient of our objective function using just two Maxwell solves each optimization iteration. In the case of the 90/10 splitter, we defined a unique figure of merit (FOM) for each arm over twenty discrete wavelength points between 1.5 μm and 1.6 μm, for three unique design fields[15] (nominal, over-etched, and under-etched), totaling 120 independent objective functions that are efficiently and simultaneously solved each optimization iteration using our TO framework. Figure 1(a) illustrates the design evolution as a function of optimization iteration and Fig. 1(b) describes the performance evolution for each arm. The final simulated broadband performance shows $\pm 0.5\%$ deviation from the nominal split (Fig. 1(c-d)), even when the device design is over-etched (Fig. 1(g)) or under-etched (Fig. 1(c)). The mean simulated insertion loss of the main coupling structure was 0.6 dB. The 50/50 and 99/1 splitters were designed to achieve similar performance.

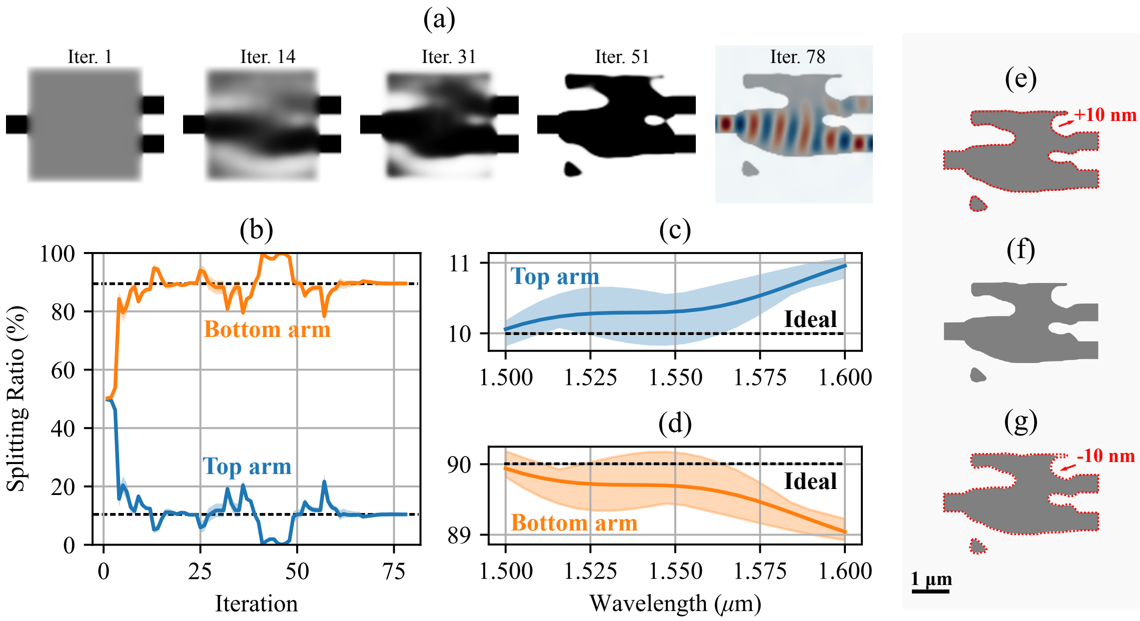

Fig. 1: Robust design process and simulated performance of the asymmetric splitter. (a) The design evolution of the splitter at iterations 1, 14, 31, 51, and 78 with the steady-state field response at λ=1.55 µm superimposed over the final device geometry. (b) The performance evolution for each arm as characterized by the respective splitting ratio. The mean broadband performance across the three different design variation is indicated by a dark orange line for the bottom arm (c) and a dark blue line for the top arm (d). The minimum and maximum worst case performance across the band is indicated by a lighter shade underneath. The under-etched (e), ideal (f), and over-etched (g) design variations with etch perturbations of 10 nm. The ideal case is outlined in red on both the under/over etched variants to highlight the minor topological differences.

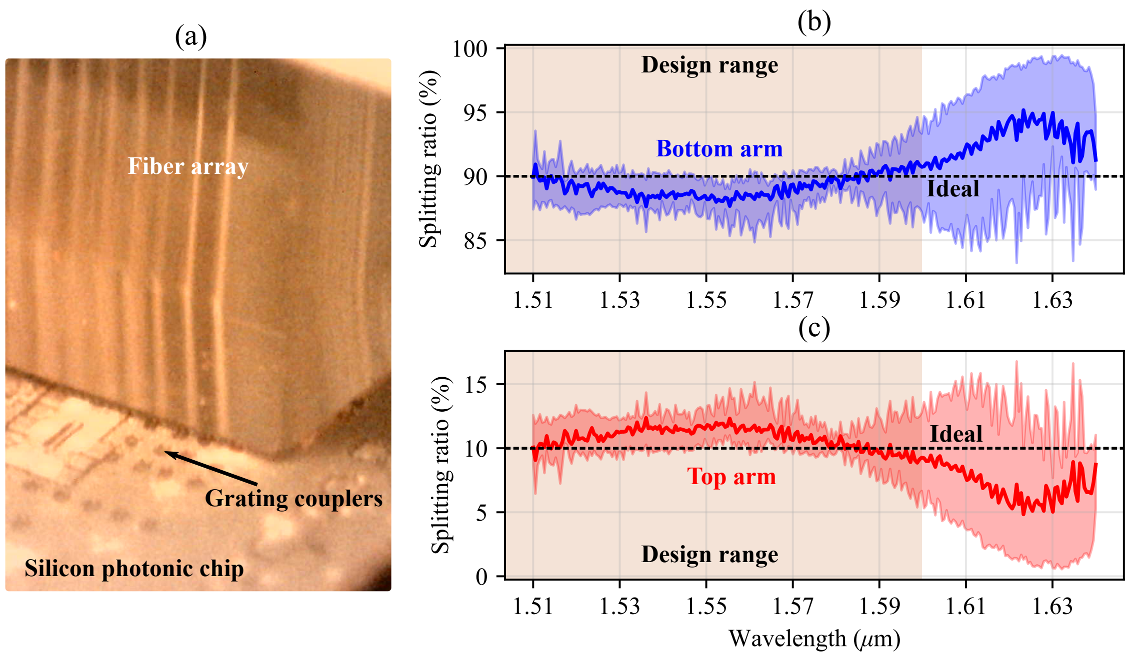

Fig. 2: Experimental splitting ratios as a function of wavelength across three devices randomly sampled from different wafers. The mean value across all three samples for each wavelength point is indicated by a dark blue line for the bottom arm (b) and a dark red line for the top arm (c). The minimum and maximum values across the three samples are depicted by a lighter shade underneath. The ideal splitting ratio (90% and 10%) is depicted by a dashed black line. Measurements were taken from 1.51 µm to 1.64 µm. Within the design range (1.5 µm-1.6 µm) the devices show ±2% variation in mean splitting ratio across the band. As expected, device performance deteriorates quickly outside the design range. Devices were interrogated using standard PDK grating couplers and a fiber array (a).

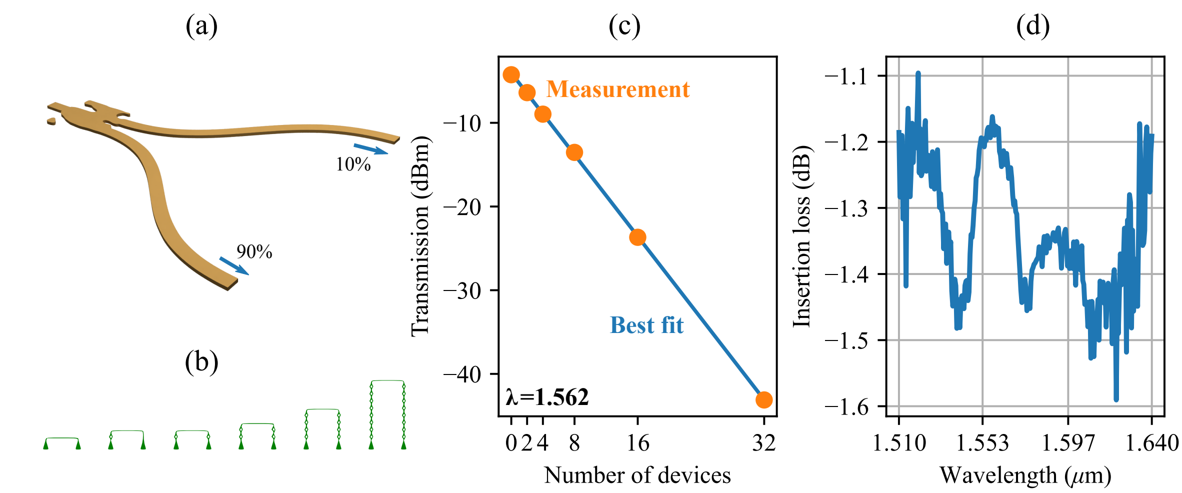

Fig. 3: Experimental loss extraction for the manufactured splitters. The final splitter design (a) was cascaded in six loopback configurations with ever-increasing device counts (0 2, 4, 8, 16, 32) (b) to more accurately extract the loss of a single device and normalize out the response of the grating couplers. The transmission of each loopback was measured and fit to a regression curve (c) who's slope corresponds to the incremental loss induced by a single device. This process was repeated at each wavelength to characterize the loss across the entire band of interest (d).

Experimental results

We characterized the devices using a standard fiber-array setup that scanned each device using PDK grating couplers for the input and output (Fig. 2(a)). We measured the broadband splitting response for each splitter (50/50, 90/10, and 99/1) using three different devices randomly sampled from three different wafers from 1.51 μm to 1.64 μm, analyzing the response both inside and outside of the designed wavelength range. Within the design range, the average measured splitting ratio across the band varies $\pm$2% for the 50/50 variant, $\pm$2% for the 90/10 variant (Fig. 2(b-c)), and $\pm$0.25% for the 99/1 variant.

The insertion loss of each device was measured using several cascaded loopback test structures containing either 2, 4, 8, 16, or 32 devices back-to-back, since the simulated insertion loss was rather small for a single device (0.6 dB). We measured the transmission of each loopback structure at each wavelength and linearly fit the resulting measurements. Figure 3 illustrates the insertion-loss extraction method along with the final estimated insertion loss of the 90/10 device (1.35 dB at λ=1.562 μm). We measured a mean broadband insertion loss of 0.8 dB and 0.7 dB for the 50/50 and 99/1 splitters respectively.

The deviation between simulation (0.6 dB) and experimental (1.35 dB) insertion loss for the 90/10 splitter may be attributed to larger variations in the small "island" located in the design's lower-left corner (Fig. 1(f)), a unique topological feature not found in the other splitter designs. Future designs might impose explicit constraints that restrict small islands or holes. Similarly, additional constraints that mitigate loss due to surface roughness[16] or sidewall-angle variation may also be warranted after further investigation.

Conclusions

Using our novel robust topology optimization framework, we successfully demonstrated the design of a 50/50, 90/10, and 99/1 power splitter for a commercial foundry platform. Our devices experimentally demonstrate devices operating over 100 nm with minimal variation over multiple wafer samples, motivating a broader exploration into new device possibilities, including interferometric and coupling structures for large-scale photonic system design.

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