[Invited] III/V-on-bulk-Si Platform: Born for DRAM, Transplanted to LiDAR

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Abstract *We overview the III/V-on-bulk-Si platform with its key process, device library, feasibility, and outlook for its applications along with its comparison to III/V-on-SOI platform. Our trial on integrating photonics into 65-nm DRAM, laser development on the bulk-Si platform, and circuit and system developments for LiDAR applications are presented.*

Introduction

The silicon(Si) industry has been striving to maintain the return on investment(ROI) of the massively established silicon manufacturing infrastructures by continuing the technology evolution widely called Moore's Law[1]. However, due to increasing challenges to maintain Moore's Law and emerging applications that are difficult to cope with existing technologies, various attempts to expand the existing complementary metal-oxide-semiconductor(CMOS) technology are in progress. Within this trend, Si photonics has been pursued for the inter-chip/board/rack interconnect bottlenecks and cost-effective novel sensors through the integration of electronic and photonic circuits on the basis of existing CMOS infrastructures[2]. From this industry perspective, silicon photonics should maximize compatibility with existing CMOS technology, but until now, it has been mostly based on specialty substrates of Si-on-insulators(SOIs) that are not widely used in volume products yet. This is presumably for rapid development in legacy-free applications, but it is obviously not optimal for the legacy-driven applications where embedding photonic circuits into the legacy chip is preferred especially in the low end. Fig. 1 conceptually illustrates the integration schemes of high and low ends over possible generations. For the performance-centric high ends, the specialty platform is allowed, and the single-chip integration could be optional. For the cost-centric low ends, however, the generic platform is preferred for the single-chip integration in the end. Towards this tight integration, the inevitable integration of III/V material has been a major challenge for the Si industry, but its commercialization has been taking off recently[3]. In this presentation, we overview the III/V-on-bulk-Si(IIIVBS) platform developed for the single-chip integration with legacies, and present its application feasibilities in 65-nm dynamic random access memory(DRAM) and light detection and ranging (LiDAR).

Process and device library

The IIIVBS process is summarized in comparison to the III/V-on-SOI(IIIVS) process in Fig. 2(a). The added key processes are the solid-phase epitaxy(SPE) of the amorphous Si in the crystallization step, and the selective III/V bonding on the SPE Si layer in the III/V bond step. Note that the burried oxide(BOX) is local in IIIVBS, while it is global in IIIVS[4].

The device-level performances are summarized in Fig. 2(b and c). The key IIIVBS devices are 1-λ laser, λ-tunable laser, semiconductor optical amplifier(SOA), and photodiode. The Si and III/V structures should be carefully co-designed and co-fabricated for the lasers and SOAs. Device details are in ref. [5]-[7]. The device library also emcompasses bulk-Si devices including modulator, photodiode, and passives[8]. The devices are mostly optimized in

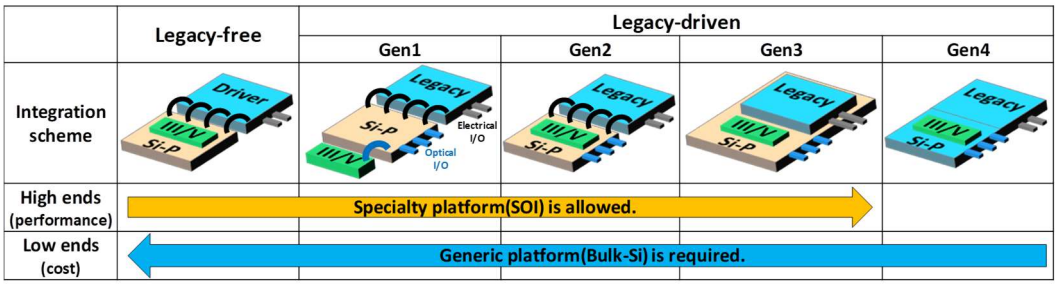

Fig. 1: Photonics integration with legacy (conceptual illustration)

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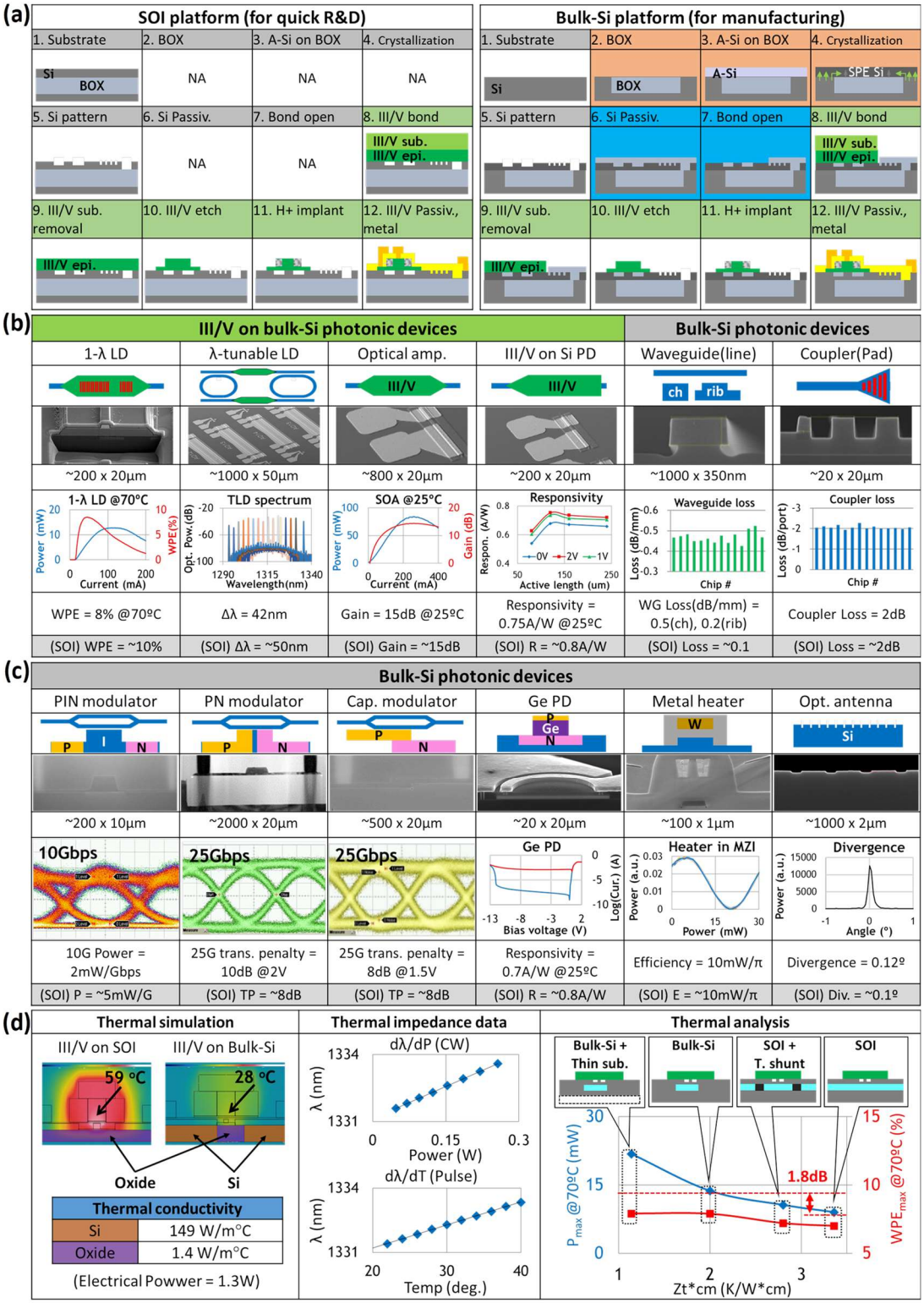

Fig. 2: Overview of IIIVBS platform, Process compared to SOI(a), Device library(b,c), Thermal advantage over SOI(d)

O-band where high-temperature laser development is facilitated thanks to its bandgap wider than C-band. Since the IIIVBS process is a superset of the IIIVS process, the device library can be converted from the IIIVBS to the IIIVS, but not vice versa.

The platform-level IIIVBS advantage compared to IIIVS is summarized in Fig. 2(d). Since the crystallinity of the SPE Si is not perfect, the IIIVBS platform inevitably suffers from the waveguide loss relatively higher than that of IIIVS. However, the local BOX in the IIIVBS platform allows the III/V layer directly contact to the Si substrate, leading to ~40% lower thermal

impedance in IIIVBS compared to IIIVS. Note that this is due to the thermal conductivity ~100x higher in Si than oxide. This lower thermal impedance translates to an optical output power at 70°C ~1.8dB higher in IIIVBS than IIIVS[7]. The IIIVBS platform is, therefore, better suited for compact photonic circuits including temperature-sensitive on-chip devices such as lasers and SOAs.

DRAM and LiDAR applications

The application-level trials with the IIIVBS platform are summarized in Fig. 3. The chronic bandwidth-capacity trade-off of the copper-based DRAM interconnect initiated the IIIVBS platform development around 2010. Co-fabrication of CMOS transistors and bulk-Si-photonics devices was achieved with ~20% process overhead[4]. At that time, IIIVBS devices were not included yet. For the optical DRAM interconnect, the photonic circuit was embedded in the periphery section of 65-nm DRAM, and showed similar performance as one fabricated from photonics-only processes. The area overhead from the embedded photonic circuit was less than 1%. In the system-level, the CPU-DRAM interconnect feeding 4 memory modules per memory channel was demonstrated, which was not possible with copper interconnects in 2010[8].

More recently, the rise of autonomous driving provides an opportunity for the IIIVBS platform to develop cost-effective chip-scale photonic sensors. In particular, LiDAR may encounter a virtuous cycle formed between cost reduction and market expansion. For the LiDAR application, the laser/SOA-integrated optical phased array(OPA) has been implemented with the IIIVBS device library temporarily applied on the SOI substrate, due to internal process issues. Insofar, decent module-level performances have been achieved, and further upgrades are ongoing[9]-[11].

Conclusions

The IIIVBS platform has been developed from the legacy-driven perspective. In the initial DRAM application, the photonic circuit was integrated into DRAM to confront the bandwidth-capacity trade-off in copper interconnects. With the IIIVBS device library completed with lasers and SOAs added, the feasibility of the chip-scale LiDAR has been achieved with decent performance and promising scalability.

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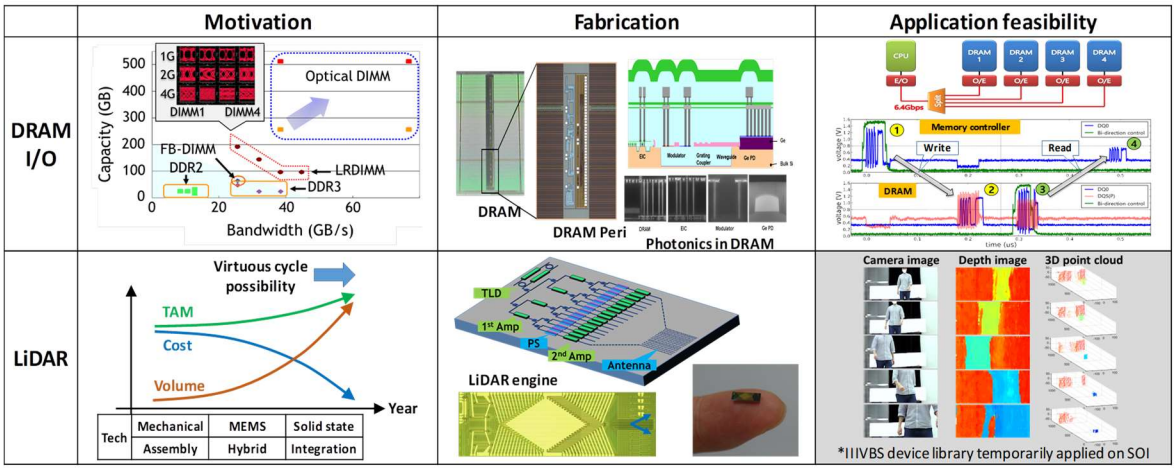

Fig. 3: Application status of IIIVBS platform