

# Packet Delay Variation Correction for Time Sensitive Networking with Frame Preemption

Silviu Adrian Sasu, Achim Autenrieth, Jim Zou, Jörg-Peter Elbers

ADVA, 82152 Martinsried/Munich, Germany, ssasu@adva.com

**Abstract** *We report a method for correcting packet delay variation (PDV) of high priority express traffic due to frame preemption. Zero PDV with low additional deterministic delay is achieved for high priority express traffic, improving synchronization in time sensitive networks.*

## Introduction

The growing traffic in mobile communication networks and emerging use cases such as augmented reality and mission-critical communication call for lower latency and better timing accuracy in future 5G networks. Therefore, Time Sensitive Networking (TSN) will play a crucial role in enabling a packet-based mobile x-haul.

The 4G fronthaul infrastructure is currently determined by the CPRI (Common Public Radio Interface) industry specification which assumes dedicated optical links. An alternative is to use ubiquitous Ethernet technology aiming at lower network cost by leveraging Ethernet's economies of scale [9]. However, in contrast to the traditional CPRI fronthaul, Ethernet suffers from packet delay variation. Particularly for user plane traffic and also for control plane traffic, a compensation of the packet and delay variation requires a play-out buffer in the radio equipment, which needs to be twice as large as the maximum delay which can occur in the network. Packet delay variation represents one of the main limitations and results in timing jitter. As buffers infer more delay to the service, jitter calls for a higher delay in order to smoothen the data flow and causes more latency to the system. Therefore, compensating packet delay variation in the transport network reduces the play.out buffer size and the overall latency for the radio signals. There is an ongoing standardization activity in IEEE 1914.3 on how to transport CPRI over Ethernet networks and an ongoing effort in investigating novel Ethernet-based fronthaul solutions [7]. However, how to optimize Ethernet to better meet stringent 5G (e.g. eCPRI [1]) timing and latency requirements is still an area of active research.

One solution enabling the fronthaul traffic synchronization between the remote radio unit (RU) and central unit (CU) is to use Synchronous Ethernet for frequency synchronization and higher layer protocols such as PTP [6] for time synchronization.

In previous work, ultra-low latency transmission with deterministic minimum latency for PTP traffic

was achieved by prioritizing PTP information and fronthaul traffic while using best-effort gap-filling for backhaul traffic [8].

In this work, we present and experimentally evaluate a mechanism for low and bounded delay Ethernet aggregation to eliminate packet delay variation and minimize additional fixed delay on high priority fronthaul traffic. Zero PDV and very low fixed delay is achieved using frame-preemption of low-priority traffic techniques. This allows longer transmission distances and simplifies the dimensioning of the fronthaul network and eventually necessary playout buffer size.

## System Description and Problem Definition

The biggest challenge of the legacy 4G/LTE Fronthaul is the strict requirements of the CPRI data streams from the CUs to the RUs. The next generation fronthaul architecture must support traffic-dependent configuration and accurate synchronization enabling radio data transmission through a packet-based aggregation network connecting RUs to the centralized CUs.

Encapsulating Radio over Ethernet (RoE) is a cost-efficient solution which can leverage existing Ethernet interfaces, and equipment, for a packet based mobile fronthaul. The adoption of Ethernet brings many advantages such as scalability, with well-established Operations, Administration and Maintenance (OAM), and ease to upgrade to higher data rates.

There are investigations within IEEE 802.1CM [2] standard working group whether IEEE 802.1Qbu-based [3] preemption could be utilized to guarantee latency and PDV requirements for Ethernet fronthaul. A time sensitive network implementation using 802.1Qbu frame preemption requires senders and receivers to support 802.1Qbu. The receiver must extract and identify express Ethernet frames on input queues while the sender, in order to ensure preferential treatment through the network, marks all the traffic frames accordingly and preempts best-effort traffic. By interrupting the transmission of best-effort frames when a deterministic high

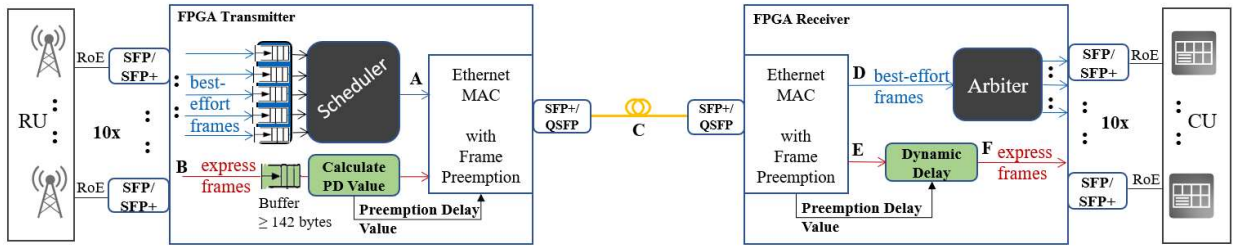


Fig. 1: System overview fronthaul implementation

priority express packet arrives, worst-case packet delay is minimized. Some Packet Delay Variation (PDV) still occurs on express traffic because preemption is only performed if at least 60 bytes of the preemptable frame have been transmitted and at least 64 bytes (including the frame CRC) remain to be transmitted. Taking the mandatory Ethernet interframe gap, preamble and delimiter into account, this results in a Preemption Delay (PD) of 142 Bytes in the worst case, and zero delay in the best case; causing a PDV of 142 bytes transmission time per hop.

### Mechanism for PDV Correction

The 142 bytes transmission time PDV caused by frame preemption can be reduced to zero by defining and transmitting a Preemption Delay (PD) delimiter header field for each express frame to the receiver as a parameter for an on-the-fly configurable dynamic delay module.

Fig. 1a illustrates the one-way data path of the proposed hardware implementation to evaluate solutions for synchronization of packet-switched fronthaul traffic. The transmitter hardware platform aggregates fronthaul traffic, which is optically connected to the receiver hardware platform connected to the CU.

On the transmitter side a one-byte delimiter header field will be inserted right after the ethernet preamble and express frame delimiter, at the beginning of the express frame data, as shown in Figure 2b. In order to avoid any throughput loss, we shorten the express frame preamble by one byte (from 7 bytes to 6 bytes), analogue to the approach described in IEEE

802.3br [4] for continuation fragments of a preemptable frame.

We observed that when preemption cannot be performed, the worst-case delay of 142 Bytes can non-deterministically affect a sequence of express packets, meaning that a sequence of express packets with gaps smaller than 142 Bytes could be non-deterministically delayed. In order to avoid this negative effect, a buffer of at least 142 bytes (worst-case preemption delay size) is required. The buffer absorbs the worst-case delay while the “Calculate PD Value” module helps keeping track of the delay introduced packet by packet. This way, whenever preemption cannot be performed, the delayed bytes are buffered, so, no backpressure can be exerted on any of the following express packets. Figure 2a illustrates an example behaviour for the preemption technique at 5 references points in the transmission system and highlights the effect of the PDV correction mechanism at reference point F. Based on the transmitted PD value, the VCD value is calculated and by delaying helps reconstruct the time period between express frames, this way, we achieve at reference point F a fixed delay of 142 bytes transmission time and zero PDV.

The calculated delay value is inserted by the TX Ethernet MAC in the PD delimiter header field as described above, extracted on the receiver side and forwarded to the dynamic delay module.

The dynamic delay module, illustrated in Figure 3 and placed between the reference point E and F in Figure 1, eliminates PDV by additionally delaying express frames with a Variable

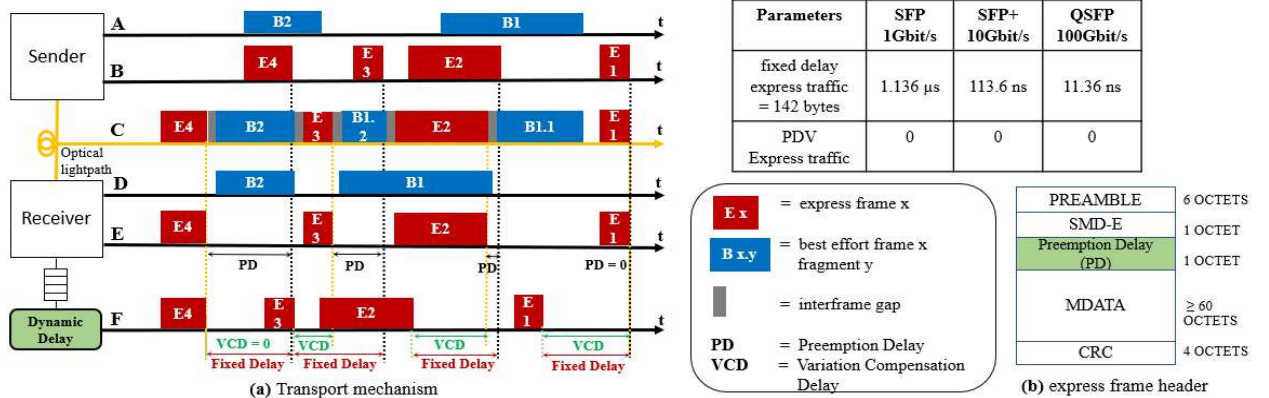


Fig. 2 (a) frame preemption with PDV correction – transport mechanism (b) express frame header layout

Compensation Delay value (VCD) (1) calculated for each express frame as

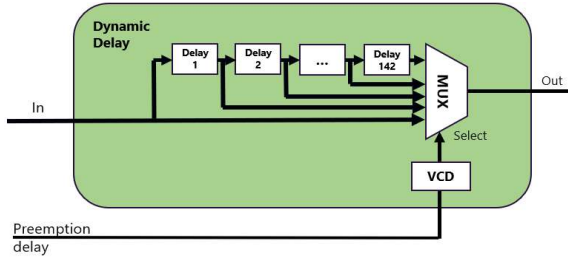


Fig. 3: Dynamic Delay

$$VCD = 142 (\text{max. preemption delay}) - PD (1)$$

The previously mentioned module applies on-the-fly and packet-by-packet an additional delay to the high-priority express packets according to the calculated variation compensation delay (VCD), value to compensate the preemption delay (PD) introduced by the preemption mechanism at the transmitter. As illustrated in Figure 3, the module consists a serial connected delay registers having outputs connected with inputs of a multiplexer receiving as a selection control signal the VCD value.

### Simulation results and discussion

To evaluate the proposed technology and its behavior, an VHDL-based frame preemption with PDV correction is implemented and examined by running hardware behavioral simulations. Independent simulation was performed with various random seed numbers. We consider two types of traffic in the communication system, express traffic and best effort traffic. We measure the performance based on various traffic intensities, packet sizes, and ratio between the two types of traffic.

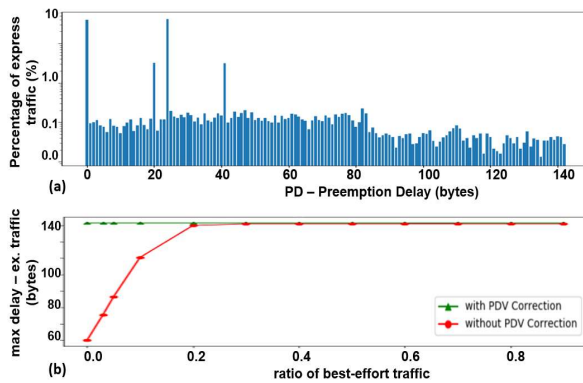


Fig. 4 (a)preemption delay distribution (b) max delay of express traffic

Figure 4a illustrates logarithmically the evaluation of the preemption delay behavior by running an FPGA hardware-based simulation using a

Linear-Feedback Shift Register (LFSR) algorithm to generate random packet lengths and packet gap sizes for both best effort and express traffic. The simulation results confirm the calculated maximum PDV of 142 bytes transmission time.

Figure 4b shows the maximum delay for express frames when express traffic constantly takes 50 percent of the total throughput and the relative load of best-effort low priority traffic is varied from 0 to 0.9 to the express traffic load. It is observed that increasing the percentage of best-effort traffic increases the probability to reach maximum preemption delay for express traffic.

### Conclusions

The presented PDV correction method achieves zero PDV with very low upper-bounded additional fixed delay for high-priority traffic. For a 100Gbit/s Ethernet aggregated fronthaul stream, it leaves 99.8μs of a 100μs fronthaul delay budget to transmission delay and packet processing, and does neither limit the maximum Ethernet frame size for both traffic types nor the priority mechanism for low-priority traffic.

### Acknowledgements

This work has received funding from the European Union's Horizon 2020 Research and Innovation Program under Grant Agreement No. 871900 (5G-COMPLETE).

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