High-speed silicon photonic modulator based on forward-biased PIN diodes and passive equalizers

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Abstract *A high-speed all-silicon photonic modulator is a key component for energy-efficient optical transceivers. This talk reviews our bandwidth enhancement technique for an all-silicon modulator using passive RC equalizers. We present 90 Gbaud NRZ and 70 Gbaud PAM4 operations of a segmented MZ modulator. The simulated performances of the optical DAC based transmitter are also discussed.*

Introduction

The strong demand for a larger data transmission capacity has continuously driven technology innovations in optical transceivers. A larger transmission density and higher energy efficiency are strongly required. State-of-art transceivers include a collaboration of high-end technologies, such as signal processing and high-speed electronic and photonic components. Silicon (Si) photonics technology has been a key technology in photonic components. Although it has been deployed as a commercial technology, further improvements in terms of the size, power and cost have been investigated through a stronger integration with electronics[1,2]. In the applications of Si photonics technology to next-generation transceivers supporting >800Gb/s, a main challenge still remains in the high-speed operation of the transmitter. Due to the saturation observed in performances of all-Si modulators, alternative approaches such as hybrid integration have been eagerly studied to overcome this limitation[3]. However, an all-Si modulator still has significant merits in terms of cost, reliability and temperature immunity. Therefore, a bandwidth enhancement technique of an all-Si modulator can be a key enabler for the next technology innovation. In this talk, we review our recent work on a bandwidth enhancement technique of an all-Si modulator using a forward-biased PIN phase shifter (PS) and a passive RC equalizer. An energy-efficient, multi-level transmitter architecture based on the optical DAC concept is also investigated for next-generation transceivers.

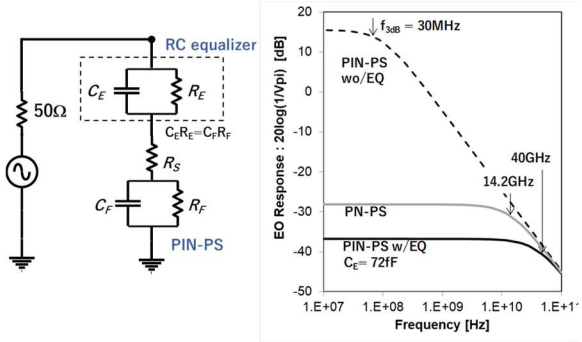

Fig. 1: Equivalent circuit of Si PIN-PS with RC equalizer (left), and calculated EO responses in 50Ω system.

High speed all-Si modulator using an RC equalizer

An operation principle of all-Si modulators is the carrier plasma effect. A Si PS generates an optical phase shift corresponding to an injected or depleted carrier into the waveguide core. Thus, an all-Si modulator and its driving circuit have to be co-designed to provide a large amount of carriers into Si PSs in high frequencies. The most popular architecture of Si transmitters is a combination of a traveling wave modulator and a large-swing current mode driver. It can drive a long Si PS with a single driver circuit. However, the modulator suffers from a large RF loss induced by a capacitance of the Si PS. It poses a severe limitation on the modulation bandwidth of the transmitter. The other candidate is a segmented architecture that cascades a number of Si PS segments driven by a small driver array. This architecture can avoid the influence of RF loss using a short lumped-electrode segments.
For a design of a lumped Si PS, there is a simple trade-off between the modulation bandwidth and efficiency. A Si PS with a smaller capacitance is advantageous for a broad modulation bandwidth. By contrast, a larger capacitance is necessary for a high modulation efficiency (small Vπ). Considerable prior works have been made to

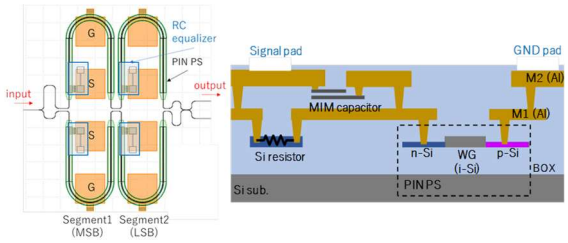

Fig. 2: Schematic structure of segmented MZ modulator. Top view (left), Cross-sectional view (right)

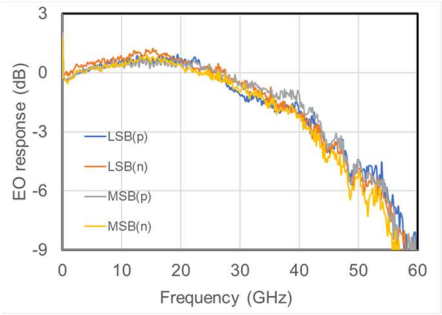

Fig. 3: Measured EO responses of segmented MZ modulator

optimize this trade-off, mostly optimizing the structure of various Si PSs[4]. We investigated a simple method to extend a modulation bandwidth that inserts a passive RC filter in a series of Si PSs as shown in Fig. 1. The time constant of an RC filter should be matched to that of a PIN PS (C_ER_E=C_FR_F) to handle a whole system as a first order RC circuit. Under this assumption, the RC bandwidth of the entire system can be increased by setting a smaller C_E than C_F. In Fig. 1, we calculated the EO responses of various Si PS models in the 50Ω system. The device lengths of all PS models are set to 500 μm. A conventional reverse-biased PN PS with a capacitance of 200 fF exhibited a 3 dB EO bandwidth of 14.2 GHz and Vπ of 25.6 V. An un-equalized forward-biased PIN PS has a very large EO response but a narrow EO bandwidth of 30 MHz due to its large capacitance of 90 pF. By inserting a passive RC filter with a C_E of 72 fF, the excess EO response at a lower frequency is suppressed, and the EO bandwidth is increased to 40 GHz. In this way, we can easily optimize the performance of a Si PS for a target operation bandwidth without consuming extra power for equalization.

To demonstrate the feasibility of this technique, we fabricated a segmented Mach-Zehnder (MZ) modulator[5]. The schematic device structure is shown in Fig. 2. The device was fabricated by a standard Si photonics process without any special process tuning. The device has two identical differential PIN PS segments, each integrating an RC equalizer designed for a 40 GHz EO bandwidth. In terms of device implementation, a precise capacitor device is a key component. We adopted a very compact (~20 μm sq.) MIM type capacitor to reduce the parasitic capacitance. Each segment has a PIN PS length of 500 μm, and the total footprint was as small as 300 x 600 μm. The measured EO responses for the two segments are shown in Fig. 3. The device exhibited very uniform EO responses with broad 3 dB bandwidths of 42.6-43.9 GHz. We also confirmed that the EO bandwidth can be controlled by changing the design of the RC equalizer[6]. The optical output

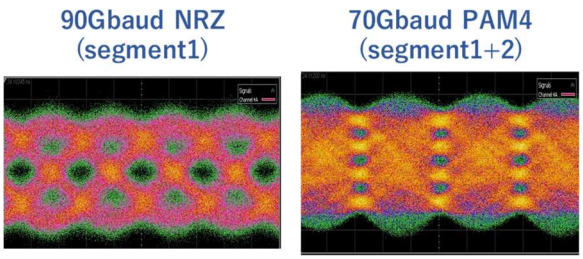

Fig. 4: Output waveform of segmented MZ modulator in 90Gbaud NRZ and 70Gbaud PAM4 operations

waveforms of the modulator are shown in Fig. 4. Two uncorrelated input data streams of PRBS11 were generated at a 92 GSa/s AWG with a raised cosine pulse shaping filter. Each signal was amplified by commercial broadband amplifiers, and then they were fed into different segments via bias-T and GSSG RF probes. In the 90 Gbaud NRZ operation, segment 1 was solely driven with a swing of 2.1 $V_{pp(SE)}$. The all-Si modulator demonstrated a clear eye opening with an ER of 1.0 dB. In the case of a 70 Gbaud PAM4 operation, we simultaneously operated both segments with 4.2 $V_{pp(SE)}$ (segment 1) and 2.1 $V_{pp(SE)}$ (segment 2). The device exhibited a good modulation waveform with an outer ER of 2.5 dB. The BER at the 70 Gbaud PAM4 operation was also measured with an 80 GSa/s DSO and an offline DSP. A conventional MMSE equalizer was applied to compensate for the limited Rx bandwidth of 32 GHz. We confirmed that the BER can be lowered below SD-FEC limit (4×10^{-2}) with our all-Si device[7].

Energy-efficient optical DAC-based transmitter integrating a CMOS inverter driver

The measurement results of a fabricated segmented MZ modulator demonstrated the feasibility of our bandwidth enhancement technique. However, its performance was strongly limited in the 50 Ω system. By reducing the output impedance of the driver, its modulation efficiency can be significantly improved while maintaining a broad EO bandwidth. A CMOS inverter driver is a suitable RF frontend for our

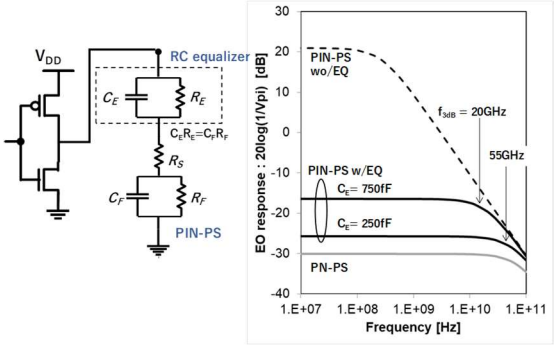

Fig. 5: Equivalent circuit and calculated EO responses of various Si PS models with CMOS inverter driver

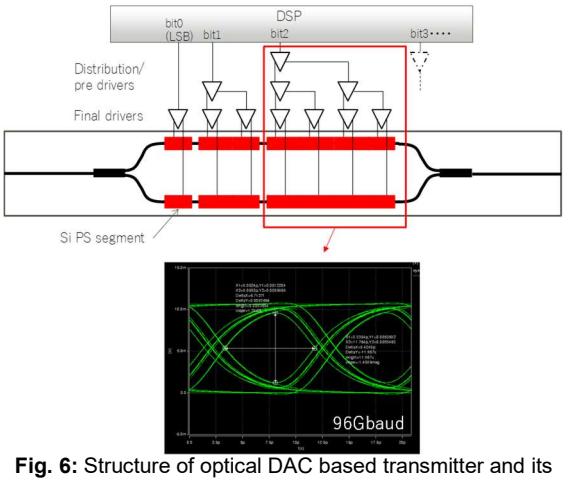

Fig. 6: Structure of optical DAC based transmitter and its simulated output waveform at 96Gbaud operation

modulator because they have a low output impedance at high and low states. In Fig. 5, the EO responses of Si PSs are calculated again by assuming a combination with CMOS inverter drivers. By reducing the output impedance of the driver, the roll-off lines of the RC responses shifted to higher frequencies. As a result, we can increase the equalizer capacitance C_E compared to the 50 Ω system case. It improved the modulation efficiency by ~10 dB. We confirmed an improved Vπ of 6.6 and 19 V for the target EO bandwidths of 20 GHz (C_E = 750 fF) and 55 GHz (C_E = 250 fF), respectively. These EO efficiencies are much better than that of a conventional PN PS (gray line). The use of a CMOS inverter driver is also advantageous for low power consumption because it consumes the current only at data transitions. The supplied current is mainly used to charge the Si PS. Thus, unwanted power consumptions at a termination or a RF transmission line can be avoided. However, due to its binary operation principle, the CMOS inverter driver is difficult to be used as a linear driver supporting multi-level modulations. For these applications, an optical DAC architecture is promising for energy-efficient transmitters. The optical DAC-based transmitter directly generates an optical analog signal from electric digital signals without using electrical DACs. Up to date, several PAM4 or 16QAM (2 bit) operations of optical DAC-based transmitters have been reported[8,9]. They can be applied to higher order modulations (larger number of bits) by increasing the number of segments.

We developed an all-Si PAM4 integrated transmitter[10]. A 28-nm CMOS driver chip was integrated with a Si segmented MZ modulator chip through flip-chip bonding. The modulator employed a passive RC equalizer for an EO bandwidth of 20 GHz (similar as C_E = 750 fF in Fig. 5). We designed a CMOS driver circuit utilizing an optical/electrical converged SPICE simulation including a nonlinear PIN PS model[11]. The transmitter exhibited a clear 56 Gbps PAM4 output waveform with an outer ER of 4.7 dB. We also confirmed a high power efficiency of 1.59 mW/Gbps. For the next step, we investigated a higher speed operation of the integrated transmitter using the SPICE simulation. We assumed an optical DAC with a binary-weight architecture as shown in Fig. 6. Both the lengths of the PS and driver sizes were scaled corresponding to the bit weight. The design of the RC equalizer was updated to C_E = 250 fF to accommodate with a 100 Gbaud-class operation. The 28-nm CMOS inverter driver circuit was also tuned to provide a larger current swing to the PIN PS. A simulated optical output waveform in the bit2 segment is shown in Fig. 6. The bit2 segment model includes a distribution circuit, a final driver, and a PIN PS with an RC equalizer. We confirmed a clear eye opening at 96 Gbaud with an optical phase swing of 0.07π. The power consumption of this segment was 35.9 mW. If we configure a 5-bit optical DAC transmitter, its total phase swing and power consumption are estimated to be approximately 0.55π and 300 mW, respectively. Note that this power consumption should be compared to a total power consumption of an electrical DAC and a linear driver. This result indicates that the passive RC equalizer technique can be a key technology to realize a high-speed, energy-efficient optical DAC that breaks future bottlenecks on the analog bandwidth and power consumption of optical transmitters.

Conclusions

We reviewed recent progresses on a bandwidth enhancement technique of an all-Si modulator toward next-generation optical transmitter. A forward-biased PIN PS integrated with a passive RC equalizer demonstrated a broad EO bandwidth up to 43.9 GHz thorough an optimization of the bandwidth-efficiency trade-off. The fabricated device exhibited good performances on 90 Gbaud NRZ and 70 Gbaud PAM4 operations. We also investigated its application to an optical DAC-based transmitter using the SPICE simulation. The simulation results successfully exhibited its feasibility to 100 Gbaud class, ultra-low-power-consumption transmitters.

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