In-plane monolithic integration of scaled III-V photonic devices

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Abstract *In this work we will discuss the use of Template-Assisted Selective Epitaxy (TASE) for the monolithic in-plane integration of active III-V photonic devices on silicon. We will show the use for high-speed InGaAs detectors, as well as for hybrid III-V/Si photonic crystal structures.*

Introduction

The integration of III-Vs on silicon is a long-standing goal because it would allow us to combine the attractive features of a low-cost, highly developed and complex silicon platform, with the added functionality of active photonic devices such as lasers and detectors.

To this end a number of approaches to grow III-V on silicon have been developed over time. Growing a planar sheet of III-V on top of silicon typically creates a poor-quality material because the two materials are not lattice matched and have different thermal expansion coefficients and polarities.

The most common method for advanced photonic applications is to bond a III-V wafer or individual III-V components on top of a Si wafer [1]. Alternatively, the growth of high-quality III-V nanowires (NWs) directly on silicon allows to achieve high-quality material [2] [3]. However, the aspect ratio of the NWs along with the vertical orientation makes the large-scale integration of more advanced devices challenging. Aspect-ratio-trapping (ART) is another epitaxial technique in which the propagation of defects is terminated in one direction by a clever design. This allows for high-quality material and nano-ridge lasers were fabricated by this method in [4], but this approach still poses restrictions in terms of device architecture, specially in the case of lateral doping.

In this work we present an approach for the local integration of III-Vs aligned with hybrid silicon features, which we refer to as Template-Assisted Selective-Epitaxy technology (TASE) [5] [6]. This technique was originally developed for electronic applications [7] and more recently extended to photonics [8], where it enables the growth of complex nanostructures. Over the course of time we have developed several embodiments depending on the desired device geometry. In this work we fill focus on planar growth on an SOI wafer. The growth extends along the surface of the wafer and includes in-situ growth of in-plane *p-i-n* doping profiles, i.e. parallel to the substrate. The high degree of control achievable in this method allows us to place contacts accurately on the scaled devices and to interact with silicon features as alignment is defined in a one-step lithographic process.

Epitaxial growth and device fabrication

A simplified schematic of TASE is shown in Fig. 1 below. In the III-V epitaxy step it is possible to incorporate either doping profiles, heterojunctions, or both in-situ, similar to vertical NW growth, but oriented along the substrate.

In some cases, one may choose to strip the template as shown here in order to place a gate electrode for example, whereas for the two types of devices which is the focus of the present work, we chose to keep the template oxide for passivation purposes. Ni/ Au contacts are implemented using conventional e-beam lithography and lift-off and is not shown on the schematic.

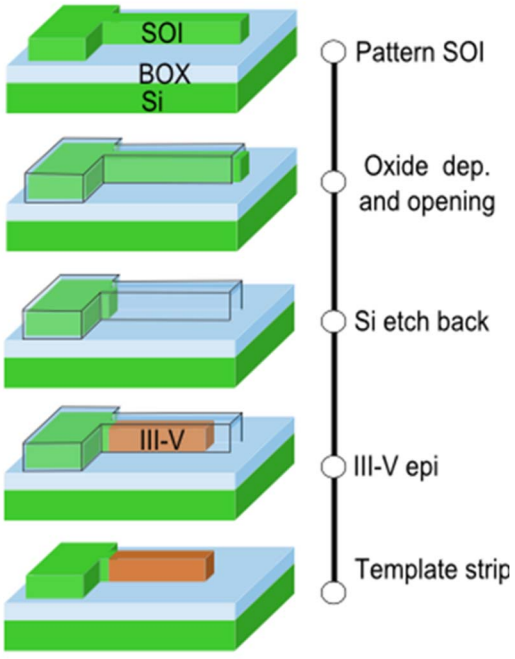

Fig. 1: Schematic of the In-plane TASE epitaxial technique. The structures are patterned in a SOI wafer. Then covered by the template oxide, which is opened at one extremity, then the silicon to be replaced by III-V material is etched back to expose a small nucleation seed. At this point the III/V material is regrown. Here, just a uniform III-V block is shown, but it might include doping profiles or heterostructures. Not shown here is the conventional contacting process. Adapted from [5].

Monolithic InGaAs photodetector

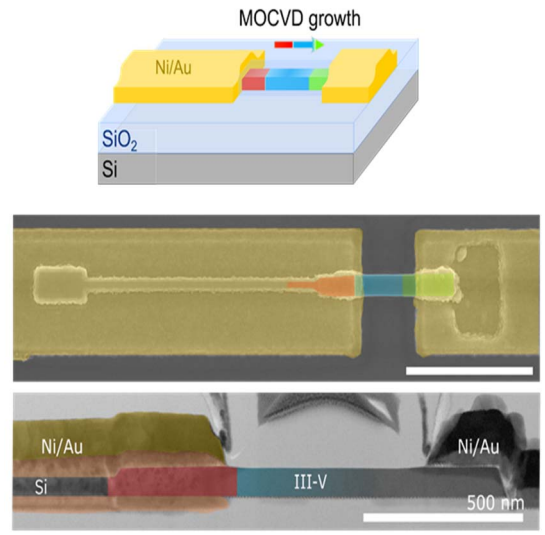

Fig. 2: Schematic of the monolithic in-plane InGaAS detector, along with false-colored top-view TEM and cross-sectional TEM of a device. The coloring indicates roughly the position of the in-situ doping profiles of the p-i-n structure. Adapted from [9].

Recently, we used TASE to demonstrate the integration of a monolithic InGaAs photodetector on Si [9], which is shown in Fig. 2. We grew 1 µm long $In_{0.5}Ga_{0.5}As$ nanostructures with a width ranging from 60 to 500 nm and with an in-situ doping profile.

The devices showed low dark currents in the range of a few A/cm^2 and responsivities up to 0.65 A/W depending on operating conditions. The measured RF response provided a f_{3dB} > 25 GHz, limited by our setup.

The spectral response is shown in Fig. 3, covering the entire telecom wavelength regime. The non-linear shape is a result of the scaled geometry and device architecture.

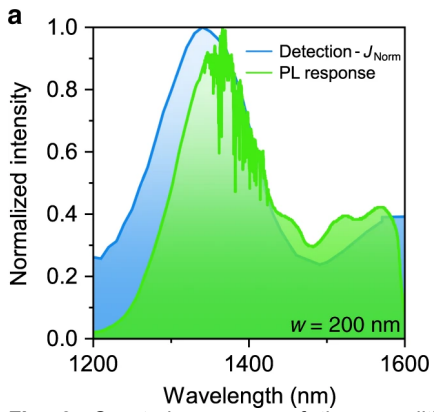

Fig. 3: Spectral response of the monolithic InGaAs photodetector from Fig. 2. In detection mode (blue) as well as the measured photoluminescence spectrum (green), adapted from [9].

Photonic crystal lasers

In addition, we have recently demonstrated a novel concept for hybrid III-V Si photonic crystals (PhC) lasers, where we exploit TASE to replace the central rods of a silicon PhC resonant structure fabricated on SOI [10]. This optimizes the overlap of the optical mode with the active gain material and reduces the loss from the mirrors. We observed PhC modes over the entire telecom band, evidence of lasing at room temperature and robustness with regards to fabrication imperfections.

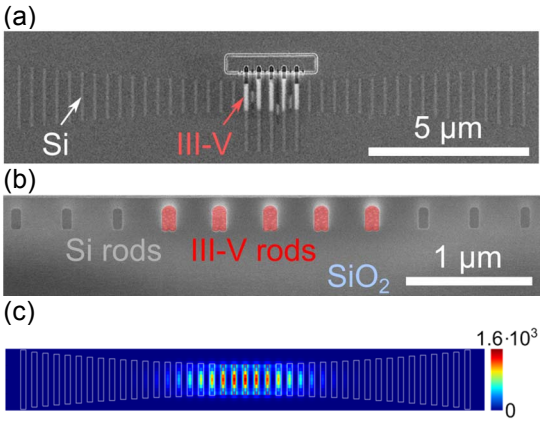

Fig. 4: (a) Top-view SEM image of a hybrid III-V silicon photonic crystal cavity, where only the central rods have been replaced by III-V material grown by TASE. (b) False colored cross-sectional TEM image of the central structure showing the hybrid approach. (c) Lumerical FDTD simulation of the optical mode. Adapted from [10].

Discussion and conclusions

Here we demonstrated the extension of TASE towards the in-plane monolithic integration approach of active III-V photonic devices on silicon and show two recent applications for light detection and emission, respectively.

The ability to create in-situ in-plane doping profiles or hetero-junctions along the device, opens for new device opportunities as it provides an alternative to implantation or diffusion doping. Furthermore, in-plane heterostructures or quantum wells orthogonal to the substrate are difficult to achieve with other growth methodologies. In-situ doping and heterojunctions is also known to work well for NW growth, where high material quality and sharp profiles might be achieved. Excellent stand-alone demonstrators have been shown via pick-and-place processing of nanowires, for single photon sources [11] as well as sub-wavelength lasers [12]. However, this method is still limited in terms of precision of NW placement and high integration densities comparable to that achievable with electronics.

Another strength of TASE as shown in the hybrid photonic crystal structures is that it allows for a seamless integration with silicon features. The III-V material replaces a previously defined silicon feature, hence there is no issue with alignment accuracy as the location is defined in a single lithographic step. It is a self-aligned process.

In the future we plan to take these concepts further by combining the two approaches to demonstrate both electrically actuated lasing, as well as waveguide coupled monolithic detectors.

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