50Gb/s Hybrid Integrated Si-Photonic Optical Link in 16nm FinFET

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Abstract *We present an EAM based single-mode optical link. The TX uses over-peaking to improve modulation efficiency and relax TIA's noise requirement. The RX uses a 3-stage TIA with T-coils to improve bandwidth. The link achieves BER<10^{-12} while consuming 4.31pJ/bit at 50Gb/s with 2dB link margin.*

Introduction

Modern data centre applications such as machine learning and high-performance computing need highly efficient distributed system architectures. Such architectures drive the demand for high-speed, low-latency serial links at 50 Gb/s and above, across multi-meter distances. In this setting, electrical signalling becomes progressively power and cost-inefficient due to frequency-dependent copper losses and channel equalization complexity. Additionally, long-reach electrical PAM-4 links require forward error correction, which increases latency. Hybrid integrated Si-Photonics links provide an appealing alternative as they are inherently free from bandwidth-distance limitations. Additionally, unlike pluggable optical modules, an integrated solution brings optics closer to the data source, further improving the bandwidth density. The packaging losses incurred in such an integration must be offset by high sensitivity and power efficiency of the optical link. In this work, we present a high-sensitivity and low-power 50Gb/s Electro-Absorption Modulator (EAM) based single-mode optical link in 16nm FinFET.

Proposed Optical Link

Fig. 1 shows the system consisting of an electrical chip (EIC) stud-bumped on top of a Si photonics chip (PIC). This allows the driver and TIA to connect to the optical modulator and photodetector (PD) with minimal parasitic effects. The PIC contains GeSi devices that work as both EAM for the TX and PD for the RX. Electrical power to the EIC is delivered through bond wires in the perimeter of the PIC, connecting it to the transceiver PCB (the "paddle card"). Light is coupled in and out of the PIC using a 12-fiber SMF array with a 250µm pitch via grating couplers.

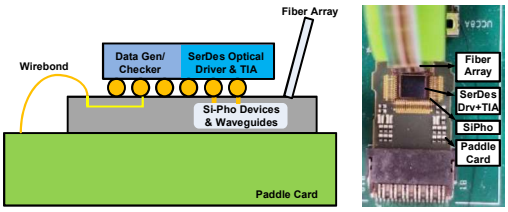

Fig. 1: Optical transciever over Si-Photonics.

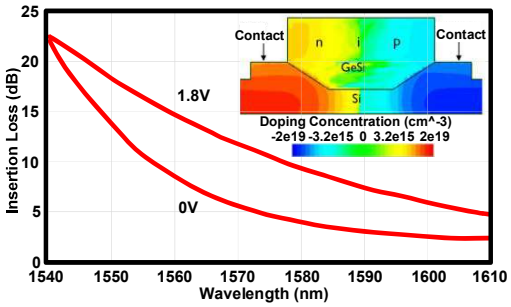

Fig. 2**:** EAM absorbption curves and p-i-n structure.

EAM Device

The GeSi based EAM device[1] used in this work, absorbs light in the C band based on the Franz-Keldysh (FK) effect. The FK effect is the distortion of the energy band (band-tilting) caused by the applied electric field. This band-tilting increases the absorption coefficient of Ge. As shown in Fig. 2, due to the electric field contrast, the EAM device has more insertion loss at 1.8 V than at 0 V. Thus, optical modulation can be achieved by electrically modulating EAM's input between 0 V and 1.8 V. In our GeSi EAM design (Fig. 2), we use a lateral p-i-n diode in reverse bias. The contacts are formed by heavily doped Si layers. The electric field contrast is generated by changing the reverse bias from 0 V to 1.8 V across the p-i-n junction. The doping profile and doping

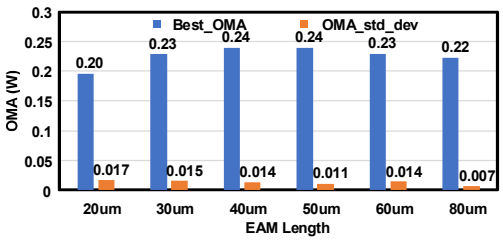

Fig. 3: EAM performance across different lengths.

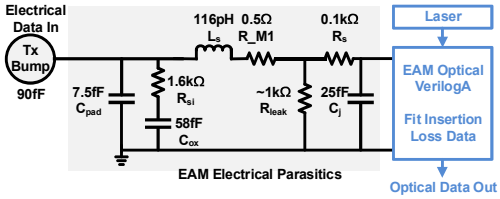

Fig. 4: EAM modelling details.

amount were optimized to ensure a strong optical overlap with the electric field, and suitably low free-carrier absorption (i.e., optical loss) due to doping. The GeSi waveguide is 600 nm wide and 50 µm long. If the EAM length is too small, then the extinction ratio is also very small and for longer lengths, the insertion loss can be excessive. Fig. 3 shows that a length of 50 µm achieves the best OMA while having smaller variations across multiple devices. The same p-i-n based EA structure is also used as a waveguide-based integrated PD. For the PD implementation, an 80 µm long EA device is chosen to achieve a responsivity of 1 A/W at 3.2 V reverse bias.

To simulate and optimize the TX driver, we need to model the EAM. The model is divided into electrical and optical sub-blocks. The electrical parasitics are described in Fig. 4. The overall electrical bandwidth is dominated by the TX bump capacitance. Because EAM is an absorption-based device, some of the optical energy gets converted to photocurrent current and it is modelled by a leakage resistor R_{leak}. Since the FK effect takes place in a sub-ps time scale, the speed of the EA modulator based on the FK effect is only limited by the RC delay. So only the voltage-dependent insertion loss is modelled while the optical dynamics are safely ignored. This modelling is achieved in verilogA. The measured insertion loss is modelled with an exponential function as IL=a*exp(-b*λ)+c. Here, a, b, and c are model parameters. Each of these model parameters is extracted from insertion loss for different input voltages (v) and are expressed in form of a second-order polynomial with respect to v. This modelling technique allows us to perform transient system-level simulation capturing the EAM device properties, including its nonlinearity.

Compared to other popular Si-based optical modulators, namely the Micro Ring Modulator (MRM) and the Mach Zehnder Modulator (MZM), the EAM has lower thermal sensitivity than the MRM and smaller size than the MZM. Owing to its small size, the EAM's capacitive load is also small. The EAM has better electro-optical bandwidth than the MRM as it is not a resonant based device. It has a moderate modulation efficiency compared to the MRM and the MZM, which necessitates a high-swing TX driver. This is described in the next section.

Transmitter Design

The transmitter is designed to provide a voltage swing of 0 V-1.8 V to improve the effective OMA of the EAM device. A cascode driver[2] is used to generate a 2× voltage swing from 0.9V and 1.8V supplies while using standard MOS devices. We modified the conventional cascode by incorporating a T-coil between the drains of the cascode devices (Fig. 5). The inductors in the T-coil increase the output impedance of the driver at higher frequencies, leading to an over-peaked response. Additionally, the T-coil ensures that the parasitic capacitance in the PMOS branch is hidden during the 1→0 transition and that of the NMOS branch is hidden in the 0→1 transition. This reduces self-loading and improves the driver's bandwidth. To compensate for EAM's nonlinearity, the data rise and fall times are independently controlled by digitally altering the effective strengths of PMOS and NMOS tail devices in the final stage of the TX. The proposed transmitter output stage

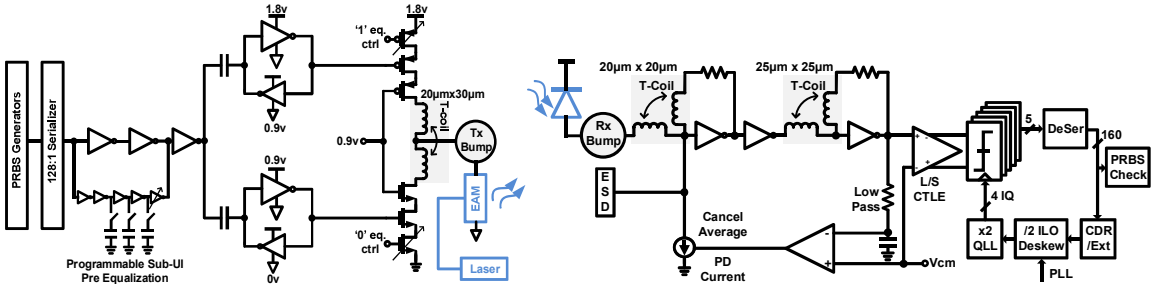

Fig. 5: TX (left) and RX (right) circuit architecture.

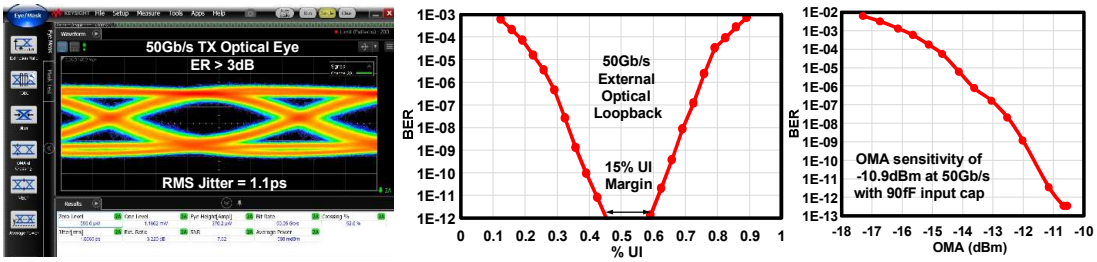

Fig. 6: Measured TX eye (left), measured bathtub curve (middle), and measured receiver sensitivity (right).

requires an upshifted logic voltage (0.9 V-1.8 V). This is achieved using an ac coupled latch. We pick a latch-based approach over passive ac coupling because it is insensitive to long sequences of zeros and ones. Fig. 5 shows the complete TX architecture. The transmitter serializes 128b data into full-rate NRZ signals without TX FIR equalization. The 4-to-1 serializer employs a quarter-rate clocking architecture. To reduce TX output jitter from clocking mismatches, phase errors of the four-phase 12.5 GHz clocks are sensed and corrected using inverter-based digital delay cell with independent control over rising and falling edges. Sub-UI deemphasis is used at the pre-driver to allow for larger fanout of the predriver stages without significantly increasing ISI induced jitter. The delay and strength of the de-emphasis is programmable to compensate for PVT variations.

Receiver Design

The most vital block in an optical RX is the TIA. It converts the small photocurrent input into an output voltage. The TIA needs to be carefully designed to meet the gain, bandwidth, and noise specifications. TIA's architecture is shown in Fig. 5. An inverter-based TIA[3] design is chosen to fully utilize the scaling benefits from 16nm technology. T-coil based bandwidth enhancement is used to reduce the number of stages of the TIA to three. The design achieves a gain of more than 1.5 KΩ with a bandwidth higher than 30 GHz in three stages. Fewer stages lead to lower power consumption. Additionally, the supply to the TIA is regulated out of a 1.2 V supply to reduce power supply noise. Apart from bandwidth, another important aspect of TIA design is its noise performance. The main source of noise is thermal noise from the first inverter. This is mainly due to noise peaking from the effective capacitance at the TIA input C_{in}. To reduce this noise contribution, a waveguide-based PD is used. Sized at only 0.6 µm×80 µm, the GeSi based waveguide PD achieves > 40 GHz 3 dB bandwidth while contributing <35 fF junction capacitance. Also, we remove the power grid under the RX bump to reduce C_{in} contribution from the EIC. Additionally, increasing g_m reduces noise so we size the first stage in such a way that g_m increases until self-loading does not become the dominant source of C_{in}. This way, we leverage the higher f_T ($\approx g_m/(C_{gs}+C_{gd})$) of 16 nm FinFET technology to reduce TIA's noise. High frequency TX peaking allows the TIA to reduce its bandwidth and improve its noise further.

The output of the TIA is connected to a single stage NMOS-based continuous-time linear equalizer (CTLE) that performs single-to-differential conversion and voltage level shifting for the next stage. The CTLE output drives five StrongArm-based slicers[4] which are clocked by four phases of a quarter-rate clock. The fifth slicer is an error slicer, which samples the peak of the input signal and is used in combination with the data samples to perform a baud-rate clock and data recovery (CDR). The quarter-rate data gets deserialized using a 4-to-128-bit deserializer and is fed to the calibration logic, CDR, and the PRBS checkers.

Measurement Results

The design[5] was fabricated in a 16nm FinFET process with a per channel active area of 0.27 mm^2 of which the TIA and TX driver occupy 8% and 5% respectively. The measured TX optical eye diagram at 50Gb/s with PRBS7 has an extinction ratio (ER) >3 dB with 1.1 ps jitter (rms) (Fig. 6). Fig. 6 also shows the measured bathtub curve of a TX to RX link in an external loopback configuration. The link achieves BER<10^{-12} for >15% UI at 50 Gb/s. The RX achieves a sensitivity of -10.9 dBm (OMA) at 50 Gb/s with an estimated input capacitance of 90 fF. High link sensitivity obviates the need for any optical amplifiers in the external loopback setup. Total electrical energy efficiency including RX, TX, and clocking, is 3.16 pJ/bit. The laser consumes an additional 1.15 pJ/bit at 50 Gb/s (10% wall plug efficiency) with 2 dB link margin.

Acknowledgements

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